



Skolkovo Institute of Science and Technology

DESIGN OF POWER CONVERTERS FOR RENEWABLE ENERGY SOURCES

Doctoral Thesis

by

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DOCTORAL PROGRAM IN ENGINEERING SYSTEMS

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I hereby declare that the work presented in this thesis was carried out by myself at Skolkovo Institute of Science and Technology, Moscow, except where due acknowledgement is made, and has not been submitted for any other degree.

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Abstract

A main challenge of the 21st century is the transition from nuclear and fossil fuels to renewable energy sources, for instance, wind, daylight, tides, waves, biomass, and geothermal heat. It is essential to guarantee affordable and reliable electrical power while also protecting the climate and the environment. Additionally, with the increase in fuel prices, investing in renewable energy electricity production is becoming more profitable than in the past, encouraging the development of new technologies. Furthermore, renewable energy sources are essential for developing societies to sustain their regional economies with easily accessible natural resources and to supply power in isolated locations. Since contemporary power converters with efficient operation and complicated implementations will enable for more efficient and optimum exploitation of renewable energy sources, these technical advancements and enhancements in the energy domain will be strongly tied to power electronics research. For linking and integrating various energy sources with a greater distribution network, power converters (also known as inverters) are crucial parts. Inverters are circuits that convert DC input voltage to symmetric AC output voltage by which both magnitude and frequency can be controlled.

The main focuses of this research are: First improving features of power converters, particularly in multilevel inverters and then Z-source converters. The initial goal of the thesis is the design of the suggested 15-level inverter. It features a revolutionary design that consists of the multilevel inverter with fewer parts, making it appropriate for applications involving industrial loads and renewable energy sources. The proposed topology includes 10 switches that can produce an output voltage with the fifteen-level and three input sources. Additionally, it can be coupled in a cascade to amplify the output voltage and level count even further. The suggested inverter's key strength is its extremely low harmonic distortion at the output voltage and current as a result of the control strategy, which is based on the nearest level control strategy for producing a high-quality output voltage. This inverter is can be used in wind turbines and solar cells. The next goal of the thesis is intended to build a

Z-source converter with improved features to cover some drawbacks of Multilevel inverter. The suggested Z-source configuration provides a very high voltage boost gain at a low shoot-through duty ratio and a high modulation index to lessen semiconductor stress. Likewise, generate a higher quality output waveform. Thus, choosing lower voltage rate capacitors can decrease the weight and installation costs. This recommended structure can also alleviate the initial inrush current issue. The steady-state analysis, impedance parameter values, and working principle of the suggested inverter are provided. To emphasize its advantages, the suggested Z-source inverter construction is further contrasted with alternative impedance source inverters. The Multilevel Inverter and Z-Source Converter are both built in the Skoltech laboratory to verify theoretical results through simulation and analysis. Experimental tests are also used to validate the established theoretical conclusions.

Keywords: Multilevel Inverters, Impedance Source Converters, High Gain Converters, Cascading Converters.

Publications

1. **Samanbakhsh, Rahim**; Ibanez, Federico Martin; Koohi, Peyman; & Martin, Fernando. A New Asymmetric Cascaded Multilevel Converter Topology with Reduced Voltage Stress and Number of Switches. IEEE Access 9, 92276–92287, 2021.
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List of Symbols, Abbreviations

ANPC - Active Neutral Point Clamped
APOD - PWM Alternate Phase Opposition Disposition PWM
CB-PWM - Carrier Based Pulse Width Modulation
CM - Common Mode
DFT- Discrete Fourier Transform
DSP - Digital Signal Processor
EMC - Electromagnetic Compatibility
FACTS - Flexible AC Transmission System
FC - Flying Capacitor
LS-PWM - Level Shifted PWM
MLI - Multi-Level Inverter
NPC - Neutral Point Clamped
PD-PWM - Phase Disposition PWM
POD-PWM - Phase Opposition Disposition PWM
PWM - Pulse Width Modulation
SDC - Separate DC Sources
SDCS - Each Separate DC Source
SHE - Selective Harmonic Elimination
SPWM - Sinusoidal Pulse Width Modulation
SVC - Space Vector Control
SVM - Space Vector Modulation
THD - Total Harmonic Distortion
VSI - Voltage Source Inverter
VSIFC - Voltage Source Inverter Flying Capacitor

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Contributions

The main contribution of the thesis:

The thesis is focused on converters, which are the bridge between the renewable energy source, particularly a DC source, and the ac grid. The main goal of the research study is to improve the way to transfer the energy from the PV panels to the grid. Particularly, the research takes advantage of the many low-voltage cells in the PV structure. The idea is to combine efficiently the cells in different ways to create a sinusoidal waveform with low distortion.

Thus, a large literature review was done to get ideas about this new concept, and the final proposal is a non-equal multiple DC input source inverter, which allows up to 15 levels and can work at the grid frequency with extremely low losses. In addition, due to the very high number of levels, the total harmonic distortion is very low, so a reduced output filter is achieved.

This proposed converter is validated in the lab and the results are published. The converter is very efficient however, the main drawback is the lack of regulation when some DC inputs or PV cells work at a lower voltage. For that reason, the research proposed a second converter, which works in series with the main one, but at lower power, so basically it compensates for the drops of the first converter. For that purpose, a high-gain converter was needed and so, a new Z-source type converter was proposed and tested. Using both converters in series high efficiency and low distortion are achieved.

To summarize the contribution is:

- A new non-equal multiple DC input source 15-level inverter with low frequency modulation, low losses and low harmonic distortion. The converter was compared with the state-of-the-art and it surpasses them all.
- A second converter was proposed in the family of Z-source types, which assists the first one and improves the voltage regulation. The converter has also high efficiency and low harmonic distortion. It has also a high gain that compensates for any voltage drop or lack of regulation of the first one.
- A series configuration of both converters, so working together they achieve excellent efficiency, very low distortion, and excellent regulation.
- All of the converters were tested in the laboratory and the results were published in conferences and journals.

Introduction

Background and Motivations

A significant challenge of the twenty-first century is the transition from nuclear and fossil fuels to renewable energy sources, for instance, wind, daylight, tides, waves, biomass, and geothermal heat [1]. Protecting the environment and the climate are equally important while ensuring reliable and affordable electrical power. In addition, since fuel prices are increasing, investing in renewable energy electricity production has become more profitable than it used to be, thus encouraging the development of new technologies. Moreover, renewable energy sources are critical for developing countries to support their local economies with readily available natural resources and provide electricity in remote areas [2]. These technological advances and improvements in the energy domain will be closely related to power electronics research since modern power converters with efficient operation and complex implementations will allow for more efficient and optimized utilization of renewable energy sources. Power converters are essential components for connecting and integrating different types of energy with a larger distribution network [3].

Due to the continued growth of renewable energy's market share, new technologies are needed in the area of power electronics, especially in grid-connected applications, where green and clean energy can be obtained in different ways [4]. The most conventional for the users is to buy electricity directly from renewable energy suppliers. Another strategy employed mainly in remote locations is the stand-alone system, consisting of renewable energy sources combined with either batteries or generators for backup. A new trend is the hybrid system, which combines conventional energy with small-scale renewable energy sources. When the energy provided by the generators is greater than the user demand, the excess is fed back into the utility network. If the renewable energy source is not able to deliver the necessary amount of energy, the conventional grid supplies the difference.

The classic configuration of a grid-connected renewable energy system consists basically of two parts [5]. The first stage is the energy supply, represented in

Figure 1(a) by a photovoltaic array and in Figure 1(b) by a wind turbine. Additionally, a power conditioner is necessary to boost the voltage generated by the photovoltaic panel and rectify the ac signal produced by the wind generator. In the output stage, an inverter is used to convert and adapt the energy accumulated in an intermediate storage element (dc-link capacitor) to be consistent with the utility grid's voltage and power quality requirements. Although the configuration of the first stage depends on the type of renewable energy interface source, the output stage is essentially the same.

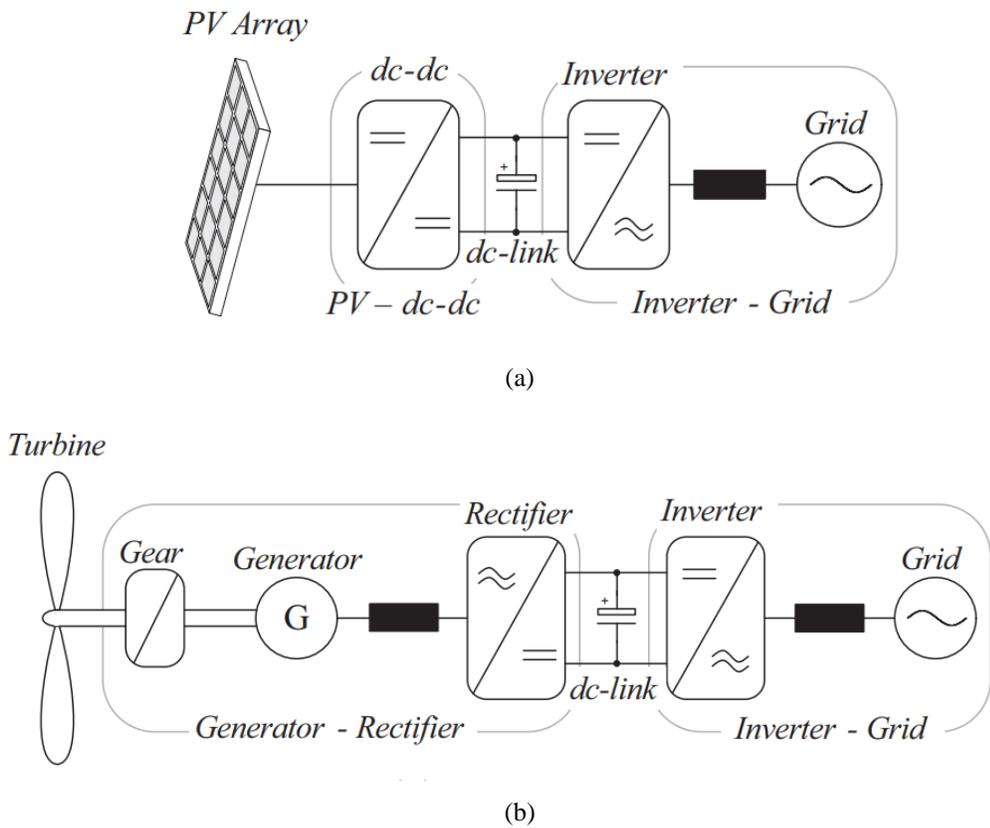


Figure 1: Typical configuration of (a) solar and (b) wind energy systems connected to the grid.

Multilevel inverters (MLIs) have been widely used for high-power, high-voltage applications. Their performance is superior to conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher

DC voltages. However, MLIs have some drawbacks, such as complex pulse width modulation control method, increased number of components, and voltage-balancing problems [6]. Among the multilevel topologies, the Modular Multilevel Converter (MMC) is one of the most promising and has received noticeable attention in academia and industry lately. The modular structure, low device ratings, easy scalability, and the possibility of using redundant cells for fault-tolerant applications are critical features of this converter [7]. Moreover, for cascaded inverters, the requirements of diodes and capacitors are also reduced.

Voltage source inverters (VSIs) have been extensively applied in various power electronic applications, such as distributed generations, energy-storage systems, and uninterruptable power supplies (UPS) [8, 9]. However, VSIs feature some limitations and constraints [10]. Firstly, the input dc voltage is higher than the ac output voltage, and for that reason, they can be characterized as buck converters. In addition, a dc-dc boost converter is needed to boost the input dc voltage to the desired dc-link voltage. By inserting the dc-dc boost converter, the complexity of the controller increases, the overall efficiency decreases and finally increases the overall cost of the inverter [11–12]. Moreover, for avoiding a shoot-through (i.e., a short circuit) between the upper (+) and the lower (-) dc-link rails, a dead time is added between the pulses, increasing the distortion in the output current/voltage waveforms. To overcome the mentioned limitations of the VSIs, the impedance source inverters (ISIs) were proposed. The first topology of the ISIs is the Z-source inverter (ZSI) which was proposed in 2002 as an alternative to the conventional VSI. The ZSI fulfills the buck-boost function in a single-stage converter by utilizing a Z-source network consisting of two identical inductors, two identical capacitors, and a diode [10, 15]. The ZSI can boost the input dc voltage to the desired dc-link voltage [16]. This in turn, increases the inverter operating range and improves its reliability since the misgating resulting from electromagnetic interference (EMI) does not affect its operation.

Main objectives of Research

This thesis focuses on improving features of power converters, particularly in multilevel inverters and Z-source converters. The first goal is to design a multilevel converter with simple control, low-frequency losses, low harmonic distortion, and high efficiency in the multilevel converter. However, the input three DC sources should be constant, if the DC voltages are reduced, output voltage will be lower. Therefore, we need to compensate this voltage drop with another converter in series. In second goal to cover this drawback, intend to build a converter with low stress on components, low inrush current and high gain in the Z-source converter. Both converters are implemented in the Skoltech laboratory, which verified theoretical outcomes both analytically and in simulation. The obtained theoretical results are also verified experimentally. Finally, the simulation results for the combination of the proposed multilevel and Z-source are added to show how the z-source compensates for the drop voltage and fixed the output voltage.

Thesis Outline

This dissertation intends to design and analyze new topology and structure and it is divided into the following seven chapters.

Introduction Provides a general introduction covering power electronics technology. This chapter covers the research background and motivations.

Chapters 1 and 2 These chapters describe the literature reviews relevant to this research topic. This chapter comprehensively investigates the previous basic topologies in multilevel inverters and Z-source converters.

Chapter 3 Provides a review of controls for mainly on Multilevel and Impedance Z-source converters

Chapter 4 Presents a new multilevel inverter for renewable energy sources. The results of simulations, experiments, and theoretical analysis are presented for 15 levels.

Chapter 5 Presents a new Z-source converter in grid-connected applications. The results of a theoretical analysis, a simulation, and an experiment are presented.

Conclusion and future work includes a summary containing the conclusions of the dissertation as well as suggestions for its future work.

Chapter 1

Literature Review of The Multilevel Inverters

Multilevel inverters

1.1 Introduction

A significant over the past few decades, multi-level power inverters have attracted researches attention dramatically. Different types of these inverters are used in high voltage and high power applications for reasons such as high-quality output waveform, low switching losses, high voltage tolerance and electromagnetic compatibility (EMC) [1-2].

The idea behind multi-level inverters is to generate a sinusoidal voltage from multiple voltage levels. Usually, these multiple levels are due to the voltage sources of the capacitors. The greater the number of such levels, the more the output waveform steps, and consequently, the resulting step wave tends to be a sinusoidal waveform with minimal harmonic distortion [3].

The final output is the result of dividing the DC-link potential into multiple phases. Therefore, each phase can switch between several voltage levels. Figure 1.1a shows a two-level inverter producing two voltage levels (Figure 1.1b) relative to the terminal M. Figure 1.1c generates a three-level voltage while the circuit in Figure 1.2e can switch between n voltage levels (Figure 1.1b).

The oldest topology for multi-level inverters was introduced in 1980 by Nabae et al. al. called Neutral-Point Clamped (NPC) [4]. This structure ensures that the voltage crossing the non-conducting switches is maintained between the diodes and connected capacitors in series.

In 1980, it was widely believed that this structure could provide tolerance twice the voltage without the need for an adaptation circuit. Therefore, it can produce a better waveform than a normal VSI waveform. Subsequently, the main structure of the NPC was proposed with a more number of levels [5-6].

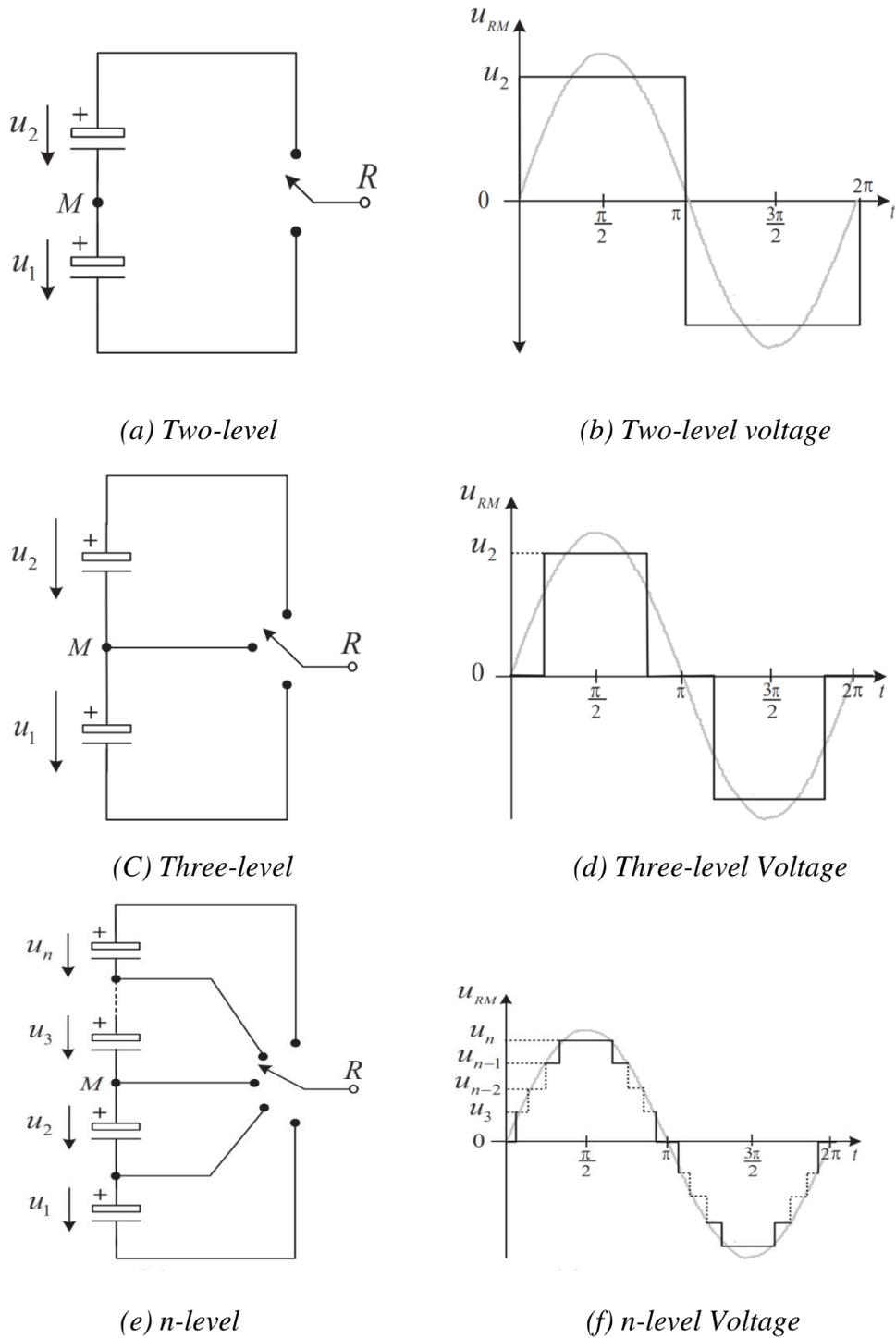


Figure 1.1 Circuit and multi-level output voltages: (a) and (b): two-level, (c) and (d): three-level, (e) and (f): n-level.

Despite all the benefits introduced, the NPC inverter faces numerous structural limitations to produce more than five levels. Although the blocked voltage of each active switch is equal to $U_{dc}/(m-1)$ (where m represents the number of levels), the reverse blocked voltage tolerance in the clamp diodes must be proportional to that level such that the clamping operation to be realized. Therefore, connecting the diodes in series is critical. But this complicates the design process and raises concerns about reliability and cost.

In 1992, Meynard and Foch proposed the Flying-Capacitor (FC) Inverter topology, in which clamp diodes were replaced by split-capacitors [7]. This structure creates a degree of freedom in the balance of split-capacitors with redundancy, and the same output voltage level is achieved by combining two or more switches. Although FC works similarly to the process of blocking clamp diodes for different voltage levels, the additional unit must be connected in series to distribute the crossing voltage stress through capacitors evenly.

In order to eliminate excess clamp elements such as diodes and capacitors and to prevent the inherent voltage imbalance, a cascaded H-Bridge inverter was proposed. The core idea of this structure is to connect single-phase H-Bridge inverters to separate power supplies in series to produce a multi-level waveform. This design was first proposed in 1990 for plasma stabilizing applications [8]. Subsequently, this method was generalized to three-phase applications such as reactive power compensation and drive applications [9]. Despite all the advantages introduced, the need for separate voltage sources has limited the applications of this structure.

In a study [10], a cascaded multi-level H-Bridge inverter with a DC source different from other sources is proposed. This multilevel topology is preferred to the multilevel asymmetric cascade structure. This strategy has been used to generate an output voltage waveform with more levels without increasing the number of energy equipment.

Recently, a new method has been introduced in which an asymmetric cascaded multi-level H-bridge inverter uses a DC power source with $n-1$ DC sources for capacitors [11-12]. The main challenge of this method is to maintain the balance of the passing voltage in each capacitor, which is created simultaneously with the sinusoidal output voltages.

In addition, in the asymmetric structure of a multi-level cascade, different voltage sources with different voltages are used. This causes the power components of the different cells to be at a separate voltage level. This feature creates a degree of freedom in the use of switch components with distinctive features such as switching speed and blocked voltage [13-14].

The proposed inverter, called the hybrid multilevel inverter, is a combination of IGBTs with fast switching capability and GTOs with high voltage tolerance capability. Switching the GTO to the main frequency requires special modulation, while IGBT is used for switching at high frequencies.

Another technique for hybrid multi-level inverters is to combine separate structures with taking advantage of each individual structure. For example, Su et al. [15], Meridoz, and Roffer [16] proposed a hybrid multilevel inverter with a DC source for a typical two-level three-phase mode with six switches and a combination of cascaded multilevel inverters. References [17-18] have also designed hybrid inverters with nine different levels for medium voltage applications. The design includes a three-level NPC IGBT three-phase inverter with a two-level IGBT single-phase inverter connected in series.

Over the past few years, the number of studies performed on hybrid inverters has increased, and various structures have been proposed. For example, Barbosa et al. In [19-20] a new structure have proposed, and called the Active Neutral-Point Clamped Inverter (ANPC), including flexible FC inverters with robust industrial NPCs to generate multi-level voltage. Multi-level inverters are classified into four

classes. Each class has its own unique topological design. The four classes include clamp diodes, FC, cascaded H-Bridge, and hybrid multi-level inverters. In the following sections, we examine each of the above structures along with their advantages and disadvantages.

1.2 Neutral-Point Clamped (NPC)

In reference [4], a three-phase m-level inverter is designed. Each terminal consists of 2 · (m-1) connected switches in series and a 1-m capacitor of link-DC type. These capacitors are charged with a voltage of $U_{dc}/(m-1)$. In balanced conditions, the maximum blocked voltage of the switches is equal to the voltage crossing through each capacitor.

Figure 1.2a reflects a phase of the structure of this three-level clamp inverter. The other two terminals have diodes, switches, and link-DC sources in common with this

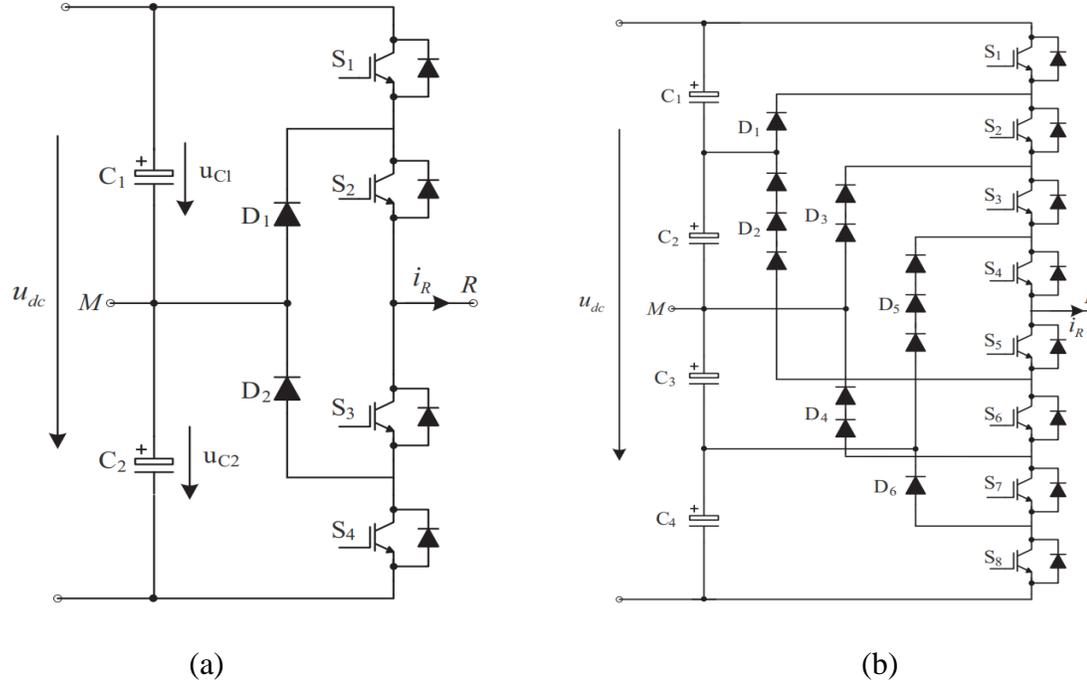


Figure 1.2 Neutral connection points. (a) Two-level, (b) Three-level.

terminal. The input voltage U_{DC} is equal to the value of the voltage divided between capacitors C_1 and C_2 . The common terminal of both capacitors that is point M represents the midpoint relative to the input voltage. The proposed topology uses the voltage of capacitors U_{C1} and U_{C2} to generate three different voltage levels at the output terminal relative to point M. The three preferred levels are $U_{dc}/2$, 0 , $-U_{dc}/2$. Obviously, a positive level $U_{dc}/2$ is created when switches S_1 and S_2 are turned on. To set the output voltage to zero switches S_2 and S_3 must be turned on, while switches S_3 and S_4 produce a voltage level of $U_{dc}/2$. Table 1.1 shows the NPC switching states. According to the table, the conduction of switch S_1 is achieved only at a voltage of $U_{RM}=U_{dc}/2$, while switch S_2 is used for switching between $U_{dc}/2$ and zero. The same logic applies to switches S_3 and S_4 in $-U_{dc}/2$ and zero.

Table 1.1 Three-level NPC output voltage and switch states

Output level	Switching States			
	S_1	S_2	S_3	S_4
$\frac{U_{dc}}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{U_{dc}}{2}$	0	0	1	1

When both switches S_1 and S_2 are on, diode D_2 generates a common and balanced voltage between S_3 and S_4 . The blocked voltage passes through capacitor C_1 by S_3 . The blocked voltage also passes through capacitor C_2 by S_4 . Therefore, the total blocked voltage is equal to half the input DC voltage. However, an imbalance in the voltage of the capacitors can cause a very large voltage in the switching components and lead to failure. As a result, it is important to control these two voltages. For the five-level topology shown in Figure 1.2b, the bus dc is divided into five distinct capacitors. This allows the inverter to create five different levels at the output and limit the blocked voltage of each switch to $U_{DC}/4$. The combination of switches in Table

1.2 synthesizes five voltage levels at the output between R and M. This NPC topology has several advantages, but in practical applications, it faces complex technical problems. For example, clamp diodes must have different block voltages. When all the bottom switches (S_7 - S_5) are on, diode D_2 requires three capacitors blocked voltages or $3U_{DC}/4$. Similarly, diodes D_3 and D_4 require a voltage of $2U_{DC}/4$ and diode D_5 requires $3U_{DC}/4$.

Table 1.2 NPC five-level output voltage and switch states

Output level	Switching States							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$\frac{U_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{U_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{U_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{U_{dc}}{2}$	0	0	0	0	1	1	1	1

We must consider this voltage rate for each diode. Several connected diodes in series are included in the circuit, as shown in Figure 1.2b. The total number of diodes required is equal to $(m-1)$. $(m-2)$. Embedding large diodes limits the number of inverter levels. Embedding of more than five diodes is impossible due to reverse voltage recovery of the diode. Another challenge of this topology is the unequal distribution of charge among semi-conductors. References [21,22] proved that the most critical operating points in NPC thermal design are located at the four boundary points, as shown in Table 1.3. For high modulation depths and inverter operating mode, the conduction of the output

Table 1.3 Semi-conductor loss distribution based on three-level NPC performance

Cases	Power Factor	Modulation Depth	Most stressed components
Case 1	1 (inverter)	1.15	Outer switches - (S_1 and S_4)
Case 2	1 (inverter)	0	NPC diodes - (D_1 and D_2)
Case 3	-1 (rectifier)	1.15	Outer switches - (D_{S1} and D_{S4})
Case 4	-1 (rectifier)	0	Inner switches - (S_2 and S_3)

switches (S_1, S_4) is achieved in the main cycle, while the conduction of the internal switches is achieved only in a short time. In these cases, some parts of the circuit get very hot while others are cold. Therefore, power losses limit the switching frequency and output power of the inverter.

1.2.1 Three-level Active NPC

To properly distribute power losses and make better use of the semiconductor, an additional pair of switches has been added to each NPC phase. This structure is known as Active Neutral-Point Clamped (ANPC) [21]. This topology connects active switches to NPC diodes. This design for one phase is shown in Figure 1.3. The inverter allows new states to be created, resulting in small losses in the semi-conductor [22]. This topology, compared to a conventional NPC, generates an active clamp of additional states and connects the output phase to the ground. This process is shown in Table 1.4 [23]. To reach level zero, a positive output current can pass through D_{a1} and S_2 like a conventional NPC inverter. It can also pass through new S_{a2} switches and non-parallel diode S_3 .

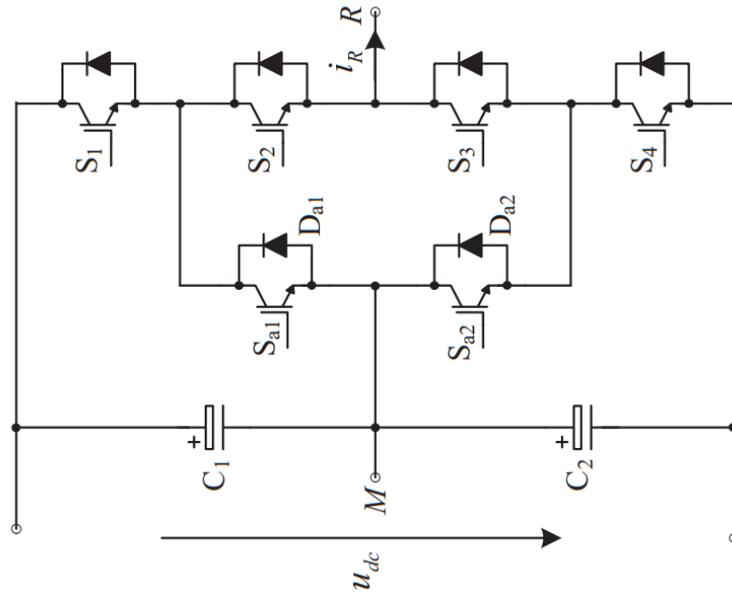


Figure 1.3 ANPC three-level topology.

Table 1.4 ANPC three-level output voltage levels and switch states

Output Level	Switching States					
	S_1	S_2	S_3	S_4	S_{a1}	S_{a2}
$\frac{U_{dc}}{2}$	1	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	0	1	1	0
0	1	0	1	0	0	1
0	0	0	1	0	0	1
$-\frac{U_{dc}}{2}$	0	0	1	1	1	0

The same behavior is observed for negative currents. The current can be connected to the ground from above or below the path. This degree of freedom can adjust semiconductor losses by choosing a different path using the appropriate modulation technique.

1.3 Flying Capacitor

As shown in Figure 1.4, a Flying-Capacitor topology with an m level can be created by a series connection of $(m-1)$ cells [24]. Each cell contains a separate pair of switches with a split capacitor. In total, $2 \cdot (m-1)$ switches, a dc power supply and $(m-2)$ split capacitors at m different levels are charged as follows:

$$\frac{U_{dc}}{m-1}, \frac{2U_{dc}}{m-1}, \dots, U_{dc}.$$

The series connection of these split capacitors with separate voltage levels provides the conditions for generating output voltage for the inverter. The connection is made when the switch on each cell is turned on. Two switches in a cell do not turn on at the same time. Also, if two connected capacitors in series with different voltage values are connected in parallel, a short circuit occurs. The combination of switches and capacitors ensures a constant blocked voltage crossing each switch according to below formula:

$$U_{S_{m-1}^h} = U_{dc} - \frac{m-2}{m-1}U_{dc} = \frac{1}{m-1}U_{dc} \quad (1.1)$$

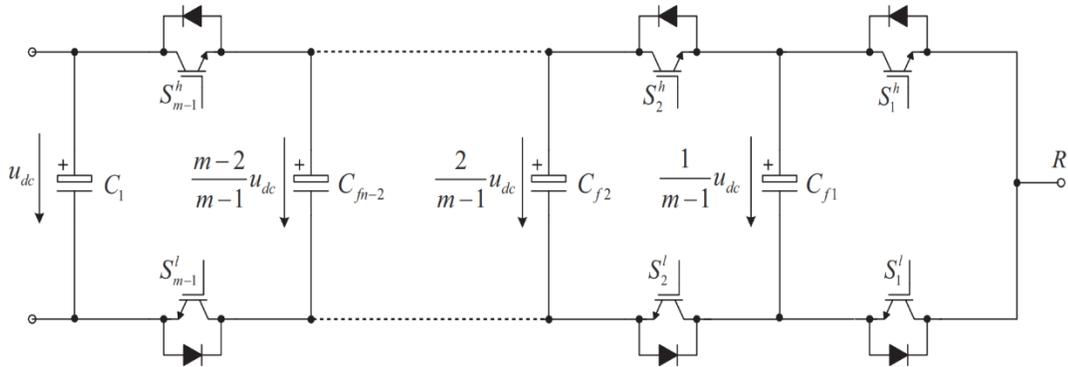


Figure 1.4 Multi-cell Flying-Capacitor topology.

An intrinsic feature of this topology is the degree of freedom in the balance of the capacitors and the redundant state in the switches.

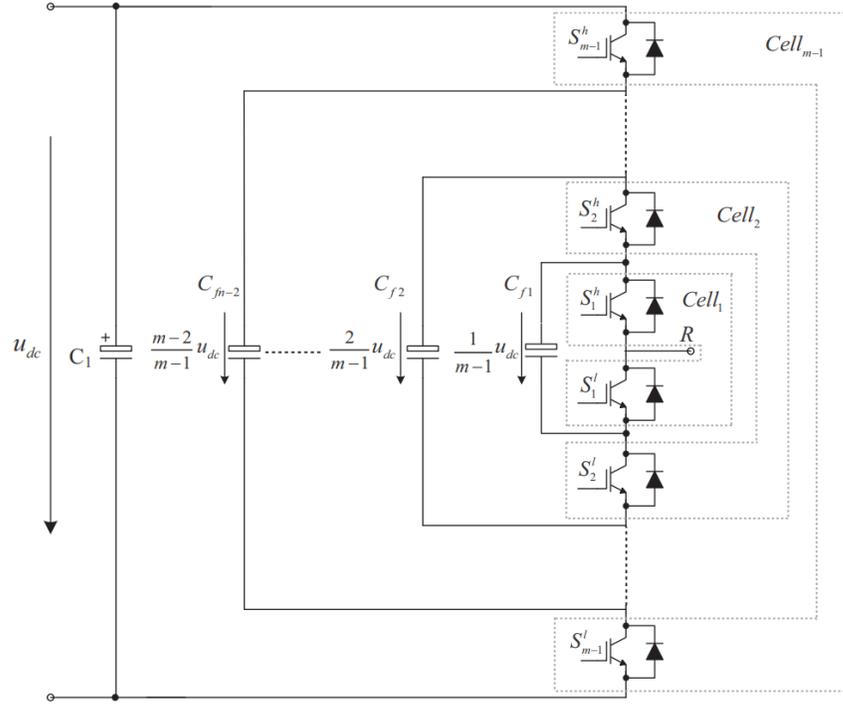


Figure 1.5 An m -level single-phase VSIFC.

The redundant voltage state produces the same output, although it has the opposite effect (charge and discharge) on the voltage crossing the capacitors. With only two cells in the structure shown in Figure 1.4, an output voltage of $U_{dc}/m - 1$ relative to the negative potential C_{f_2} (when one of the switches S_2^h and S_1^1 is turned on) is generated.

$$U_R = \frac{2}{m-1}U_{dc} - \frac{1}{m-1}U_{dc} = \frac{1}{m-1}U_{dc} \quad (1.2)$$

Or by switches S_1^1 and S_2^h :

$$U_R = 0 + \frac{1}{m-1}U_{dc} = \frac{1}{m-1}U_{dc}. \quad (1.3)$$

Although the current flows through the capacitor in the opposite direction, selecting the appropriate state in line with the output current controls the voltage crossing the capacitors. Multi-cellular representation also enables simple topological

analysis. Usually, the Flying-Capacitor VSI is similar to the single-phase circuit shown in Figure 1.5.

For the three-level case ($m=3$) shown in Figure 2.6a, the inverter produces a three-level output voltage relative to the midpoint M. Also, for the voltage level $U_{dc}/2$, the switches S_1^h and S_2^h must be turned on..

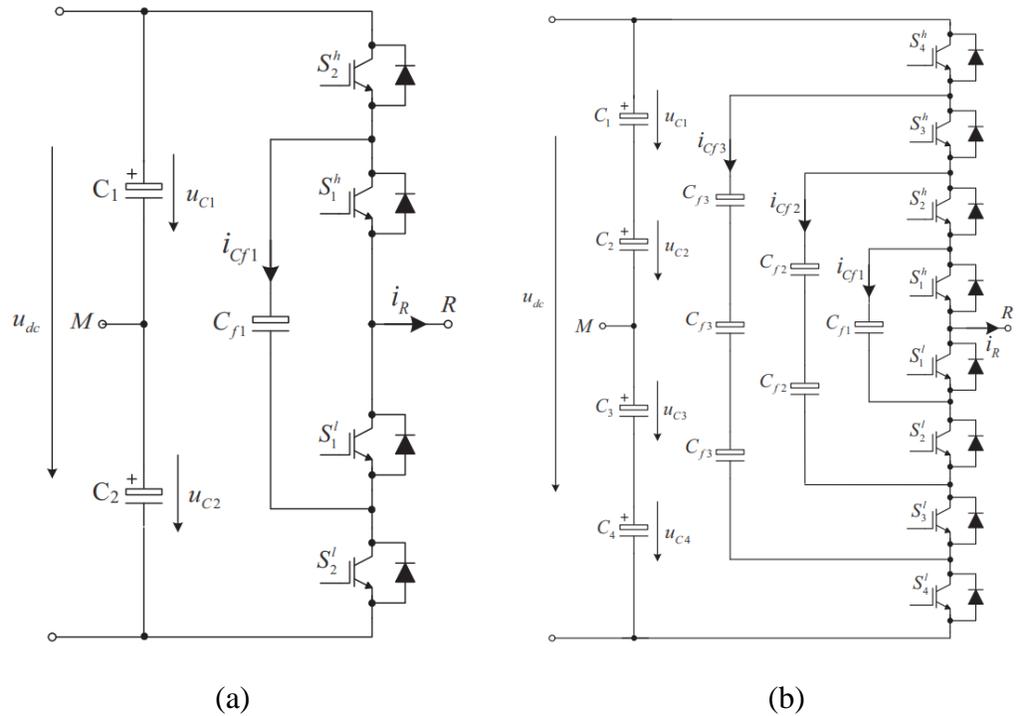


Figure 1.6 Flying Capacitor (a) three-level (b) five-level.

Table 1.5 Three-level FC inverter output voltage levels, switch states and FC output current

Output Level	Switching State				Current of C_{f1}
	S_1^h	S_2^h	S_1^l	S_2^l	
$\frac{U_{dc}}{2}$	1	1	0	0	0
0	1	0	1	0	$-i_R$
0	0	1	0	1	i_R
$-\frac{U_{dc}}{2}$	0	0	1	1	0

For negative output voltage $-U_{dc}/m$, switches S_1^l and S_2^l , must be turned on. For realizing zero level, all switches S_1^l, S_2^l, S_1^h and S_2^h must be turned on. This redundancy is used to balance the floating capacitor C_{f1} . According to the current passing through the terminal R, the first pair produces a negative current (discharge) on the floating capacitor, while the second pair produces a positive current (charge), which is reflected in Table 1.5

For the topology shown in Figure 1.6b, a large number of additional switch states increase flexibility. The output voltage relative to the midpoint (M) can be generated according to the following switching states.

- 1) For voltage level $U_{RM} = U_{dc}/2$, all top switches S_1^h, S_4^h must be on.
- 2) Specifically for the voltage level $U_{RM} = U_{DC}/4$, there are four combinations:

- $S_4^h, S_3^h, S_2^h, \text{ and } S_1^h - U_{RM} = \frac{U_{dc}}{2} - \frac{U_{dc}}{4}$
- $S_3^h, S_2^h, S_1^h, \text{ and } S_4^h - U_{RM} = -\frac{U_{dc}}{2} + \frac{3U_{dc}}{4}$
- $S_4^h, S_2^h, S_1^h, \text{ and } S_3^h - U_{RM} = \frac{U_{dc}}{2} - \frac{3U_{dc}}{4} + \frac{2U_{dc}}{4}$
- $S_4^h, S_3^h, S_1^h, \text{ and } S_2^h - U_{RM} = \frac{U_{dc}}{2} - \frac{2U_{dc}}{4} + \frac{U_{dc}}{4}$.

- 3) For voltage level $U_{RM} = 0$, there are six combinations:

- $S_4^h, S_3^h, S_1^l, \text{ and } S_2^l - U_{RM} = \frac{U_{dc}}{2} - \frac{U_{dc}}{2}$
- $S_2^h, S_1^h, S_3^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{U_{dc}}{4}$
- $S_4^h, S_2^h, S_1^l, \text{ and } S_3^l - U_{RM} = \frac{U_{dc}}{2} - \frac{3U_{dc}}{4} + \frac{2U_{dc}}{4} - \frac{U_{dc}}{4}$
- $S_4^h, S_1^h, S_2^l, \text{ and } S_3^l - U_{RM} = \frac{U_{dc}}{2} - \frac{3U_{dc}}{4} + \frac{U_{dc}}{4}$
- $S_3^h, S_1^h, S_2^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{3U_{dc}}{4} - \frac{2U_{dc}}{4} + \frac{U_{dc}}{4}$
- $S_3^h, S_2^h, S_1^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{3U_{dc}}{4} - \frac{U_{dc}}{4}$.

- 4) For voltage level $U_{RM} = -U_{dc}/4$, there are four combinations:

- $S_4^h, S_1^l, S_2^l, \text{ and } S_3^l - U_{RM} = \frac{U_{dc}}{2} - \frac{3U_{dc}}{4}$
- $S_1^h, S_2^l, S_3^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{U_{dc}}{4}$
- $S_1^h, S_2^l, S_3^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{2U_{dc}}{4} - \frac{U_{dc}}{4}$
- $S_3^h, S_1^l, S_2^l, \text{ and } S_4^l - U_{RM} = -\frac{U_{dc}}{2} + \frac{3U_{dc}}{4} - \frac{2U_{dc}}{4}$

- 5) For voltage level $U_{RM} = -U_{dc}/2$, all bottom switches S_1^l, S_4^l must be on.

Table 1.6 Five-level FC inverter output voltage levels, switch states and FC output current

	Switching States								i_{CF1}	i_{CF2}	i_{CF3}
	S_4^h	S_3^h	S_2^h	S_1^h	S_1^l	S_2^l	S_3^l	S_4^l			
$\frac{U_{dc}}{2}$	1	1	1	1	0	0	0	0	0	0	0
$\frac{U_{dc}}{4}$	1	1	1	0	1	0	0	0	i_R	0	0
	0	1	1	1	0	0	0	1	0	0	$-i_R$
	1	0	1	1	0	0	1	0	0	$-i_R$	i_R
	1	1	0	1	0	1	0	0	$-i_R$	i_R	0
0	1	1	0	0	1	1	0	0	0	i_R	0
	0	0	1	1	0	0	1	1	0	$-i_R$	0
	1	0	1	0	1	0	1	0	i_R	$-i_R$	i_R
	1	0	0	1	0	1	1	0	$-i_R$	0	i_R
	0	1	0	1	0	1	0	1	$-i_R$	i_R	$-i_R$
	0	1	1	0	1	0	0	1	i_R	0	$-i_R$
$\frac{U_{dc}}{4}$	1	0	0	0	1	1	1	0	0	0	i_R
	0	0	0	1	0	1	1	1	$-i_R$	0	0
	0	0	1	0	1	0	1	1	i_R	$-i_R$	0
	0	1	0	0	1	1	0	1	0	i_R	$-i_R$
$\frac{U_{dc}}{2}$	0	0	0	0	1	1	1	1	0	0	0

Table 1.6 shows all possible combinations of switches to generate a five-level waveform and corresponding floating capacitor currents. Positive current and negative current charge and discharge the respective capacitor, respectively.

To have different voltage levels on floating capacitors, each m-level inverter needs $(m-1) \cdot (m-2)/2$ clamp capacitors in each phase. As a result, as with the clamp diode topology, the implementation of the FC inverter is limited to a large level, as a large number of capacitors must be connected in series. The five-level method is reflected in Figure 1.6b.

1.4 Cascaded H-bridge structure

This topology is based on the connected n cell in series. It includes a single-phase H-bridge inverter and a separate DC source [9-10]. The number of levels (m) is calculated as a fraction of isolated cells based on the relation $m=2n+1$. For example, a five-level cascaded cell contains two cells. Each cell has an H-bridge inverter and an isolated DC source.

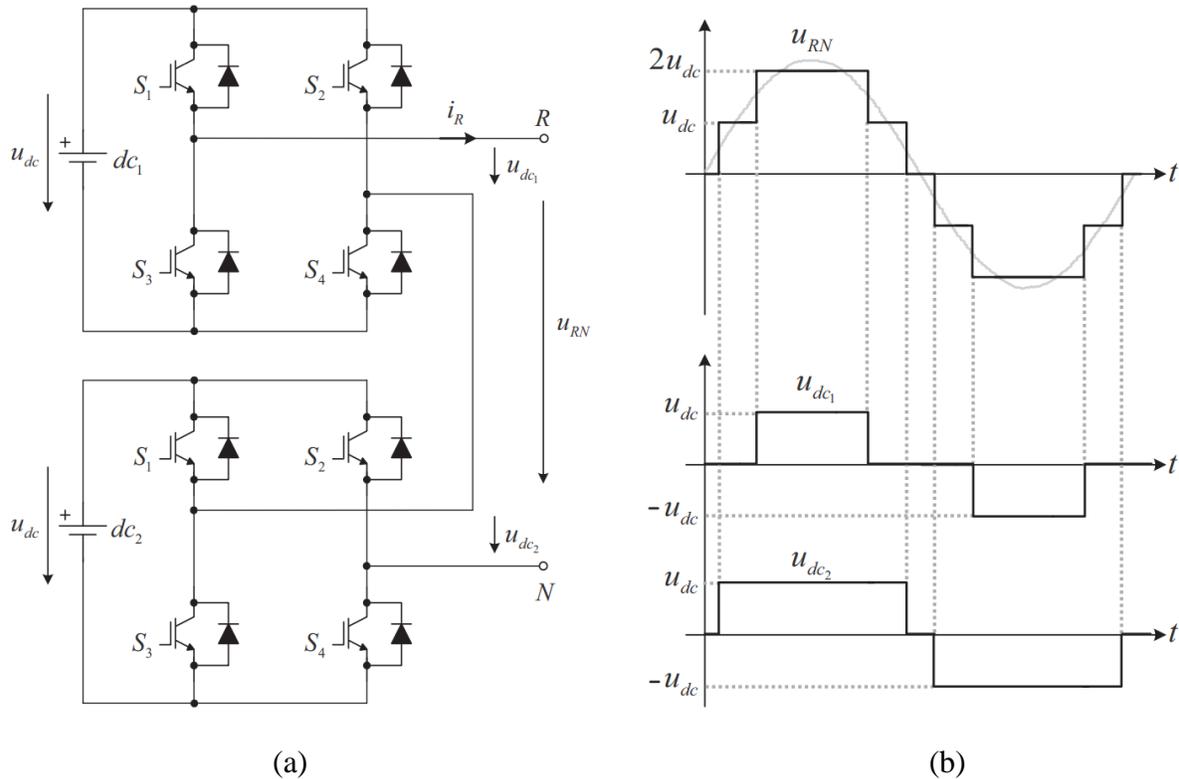


Figure 1.7 Five-level symmetric structure (a) topology (b) output voltage.

Depending on the combination of switches, each single-phase H-bridge produces three distinct voltage levels at the output. To generate a positive voltage U_{dc} , switches S_1 and S_4 must be on. To generate a negative voltage U_{dc} , switches S_2 and S_3 must be on. To generate zero voltage, switches S_1, S_2 or S_3, S_4 must be on. The resulting voltage is equal to the sum of the output voltages of the single-phase H-bridge $U_{RN}=U_{dc1} + U_{dc1} + \dots + U_{dcn}$.

Figure 1.7a shows two single-phase H-bridge inverters with a series connection. Each inverter has a switch structure and a DC voltage source. The voltage of the five-level output phase, i.e. $(0, \pm U_{dc}, \pm 2U_{dc})$ is equal to the sum of the output voltages of the two H-bridge inverters $U_{RN} = \pm(U_{dc1} + U_{dc2})$, as shown in Figure 1.7b.

The main advantage of this topology compared to other topologies such as NPC and Capacitor-flying is the reduced number of components to achieve the same level. It is also not necessary to install robust operational elements. In addition, this topology makes it possible to expand the level. The structure of each level can be similar to a single cell containing a single-phase H inverter. As a result, an additional level or cell can be added to the modular system. Despite the stated advantages, the need to embed multiple isolated DC sources limits the use of such a structure. An alternative to this is to use a secondary transformer or even multiple transformers, which in turn complicate the circuit. Another solution for electric vehicle applications is the use of renewable energy sources such as fuel cells, photovoltaic cells and biomass to produce DC.

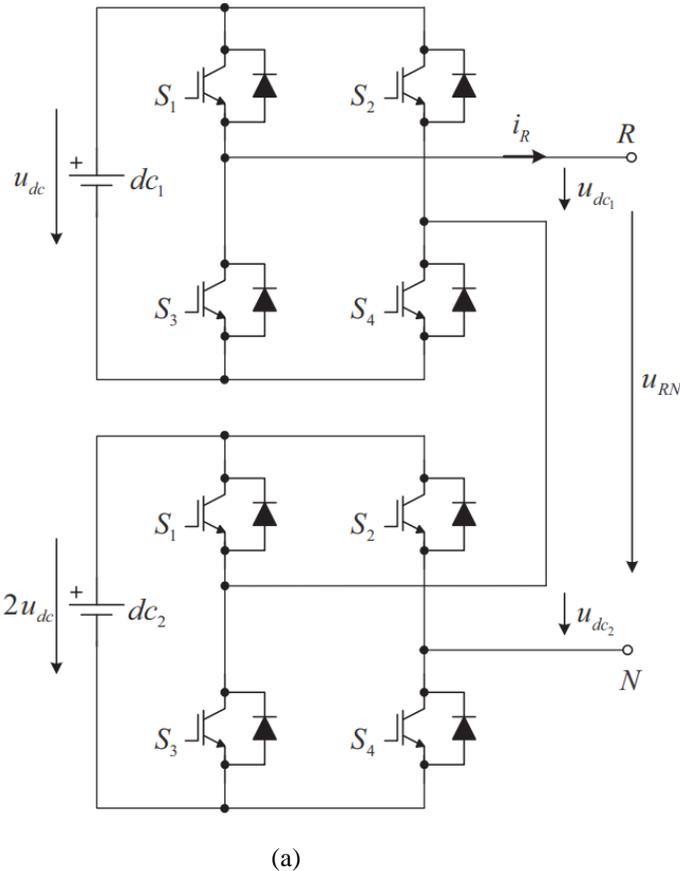
1.4.1 Asymmetric cascaded H-bridge

Another solution to reduce dc sources to produce the same levels is to use asymmetric dc voltage sources [11]. This class of inverters is called asymmetric cascaded multi-level inverters. Their circuit topology is exactly the same as symmetric cascaded inverters, but there are slight differences in the levels of voltage dc power supplies.

According to the previous discussions, the common symmetric H-bridge topology has n levels with exactly the same DC voltage in each phase and produces $2n + 1$ levels of different voltage in each output phase. Using asymmetric voltage sources DC, the number of output levels can be increased up to $(2^{n+1} + 1)$. Also, the number of voltage DC levels multiplied by two can be changed as $(u, 2u, 4u, \dots, 2^{n-1}u)$. The structure reflected in figure 1.7 has two single-phase H-bridge inverters. This structure is designed to produce five levels of output voltage but

can also produce seven levels of output voltage if asymmetric DC voltage sources are replaced by symmetric sources. This replacement is shown in Figure 1.8.

A seven-level output waveform can be achieved using two distinct patterns by combining the output voltages of H-bridge inverters (Figures 1.8b (and) 1.8c). Opening and closing the switches of the first H-bridge in time can produce an output voltage U_{dc1} equal to $+U_{dc}$, zero and $-U_{dc}$. At the same time, the output voltage U_{dc2} can be equal to $+2U_{dc}$, 0 , $-2U_{dc}$.



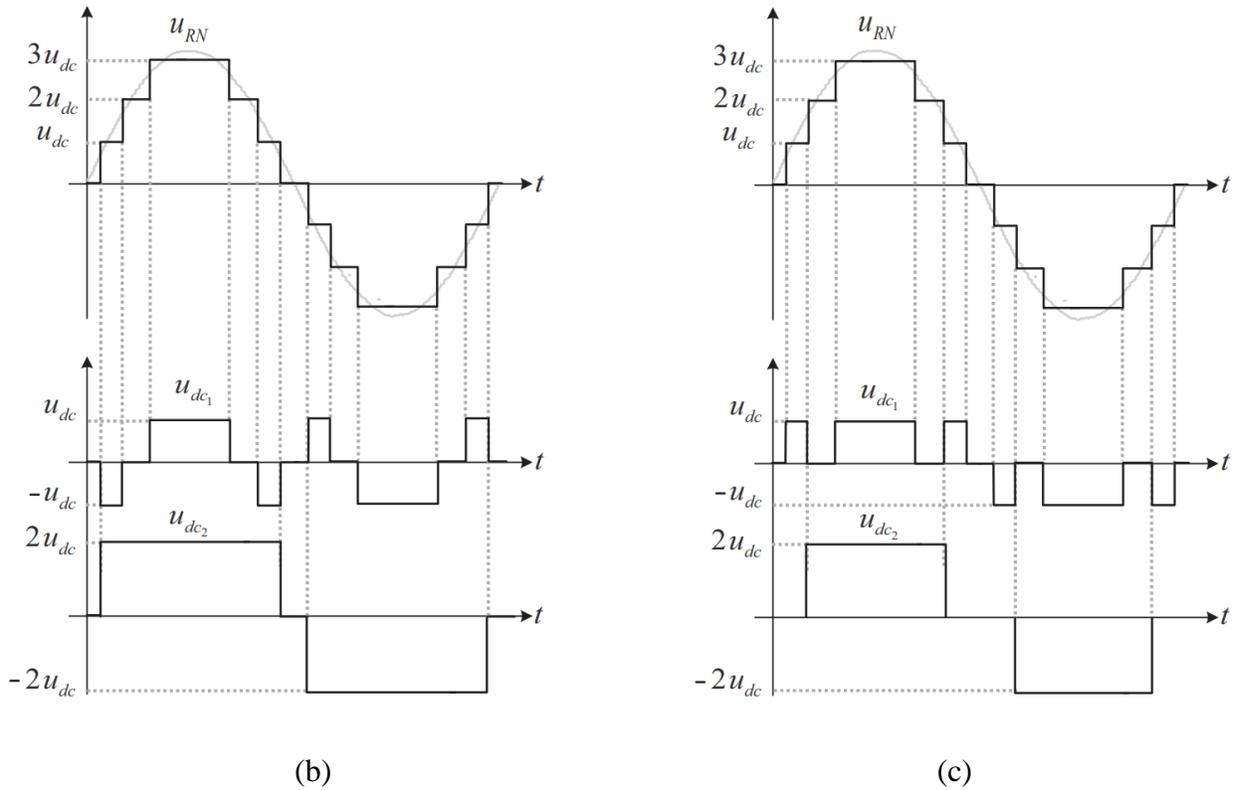


Figure 1.8 Asymmetric cascaded H-bridge (a) topology (b) first switching state (c) second switching state.

Table 1.7 Output voltage levels of Asymmetric cascaded H-bridge with single-phase single dc power supply, switches states

Output level	First switching state		Second switching state	
	U_{dc1}	U_{dc2}	U_{dc1}	U_{dc2}
0	0	0	0	0
U_{dc}	$-U_{dc}$	$2U_{dc}$	U_{dc}	0
$2U_{dc}$	0	$2U_{dc}$	0	$2U_{dc}$
$3U_{dc}$	U_{dc}	$2U_{dc}$	U_{dc}	$2U_{dc}$

As a result, the sum of the output voltages of the two cascaded inverters ($U_{RN}=U_{dc1}+U_{dc2}$) can produce seven distinct voltage levels, namely $\pm 2U_{dc}$, $\pm 3U_{dc}$, $\pm U_{DC}$. Two structures are shown in Figures 1.8b and 1.8c and are summarized in table 1.7. Due to the symmetry of the switching patterns, only the first quarter of the main cycle is investigated. Both sequences (except the redundant section) in level $-U_{dc}$ are

similar. Now we have two different combinations: Figure 1.8b $U_{RN} = -U_{dc} + 2U_{dc}$ or $-U_{RN} = U_{dc} + 0$ (Figure 1.8(c)).

1.4.2 Asymmetric cascaded H-bridge with single dc power supply

The presence of additional switching states in asymmetric cascade inverters provides a degree of freedom to reduce the number of dc power supplies required. Reference [11] uses a single power supply as the first dc source, and (n-1) another DC source has been replaced by DC capacitors. A specific control strategy is required to ensure the balance of DC voltage levels for each capacitor. A seven-level cascaded inverter with a single DC power supply is shown in Figure 1.9. At the same time, the top H-bridge inverter is powered by a dc capacitor (its controlled voltage is U_{dc}).

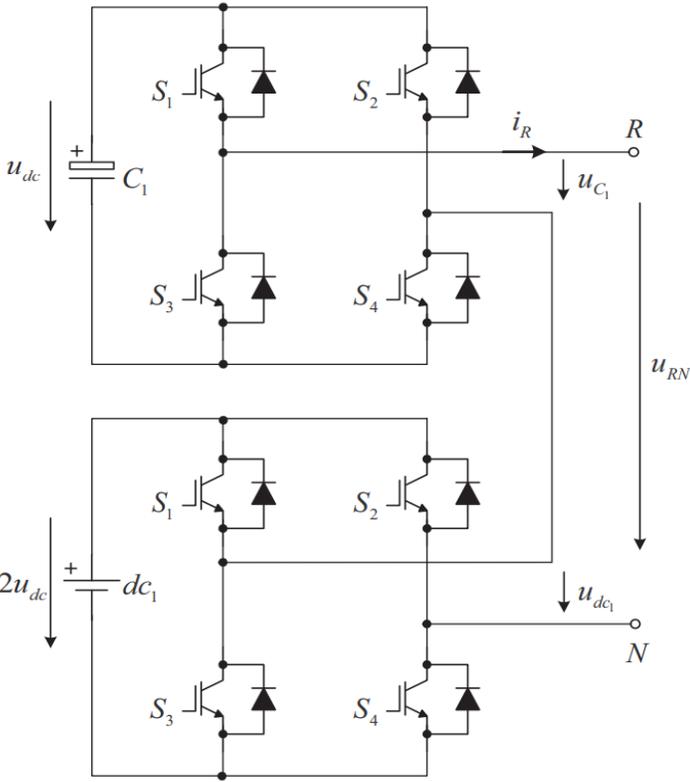


Figure 1.9 Asymmetric cascaded H-bridge with single dc power supply.

Table 1.8 Capacitor voltage difference ($\Delta U_{c1}=u_{dc}-u_{c1}$) and Output direction (positive or negative)

ΔU_{c1}	i_R	U_{dc1}	U_{c1}	$U_{RN} = U_{dc1} + U_{c1}$
-	-	$-U_{dc}$	$+2U_{dc}$	$-U_{dc} + 2U_{dc}$
-	+	U_{dc}	0	$U_{dc} + 0$
+	-	U_{dc}	0	$U_{dc} + 0$
+	+	$-U_{dc}$	$+2U_{dc}$	$-U_{dc} + 2U_{dc}$

To produce an asymmetric seven-level cascade, the output voltage equal to U_{dc} can be generated by applying $+U_{dc}$ or $-U_{dc}$ by a high H converter. This feature makes it possible to charge or discharge the capacitor based on the direction of the output current R. Therefore, a suitable switching sequence capable of regulating the capacitor voltage can be selected based on the difference between the capacitor voltage of the capacitor and the direction of the output current (positive or negative). How to choose the output (positive or negative) in Table 1.8 is presented. A negative signal means the capacitor should be discharged, and the current should be directed to the inverter. A positive signal means the capacitor must be charged, and current must flow out of the inverter. If the capacitor voltage U_{c1} is less than the desired value ($\Delta U_{c1}=+$) and the current flows out of the inverter ($i_R=+$), the modulator must combine the high H-bridge output voltage (equal to $-U_{dc}$) with the low H-bridge output voltage (equal to $U_{dc}=+2U_{dc}$) to produce a voltage equal to $U_{RN}=U_{dc}$ at the output and to charge capacitor C_1 .

1.5 Asymmetric Hybrid Multi-Level Inverters

A new type of multi-level topology called asymmetric hybrid multilevel inverters plays the role of asymmetric dc source in asymmetric cascaded inverters.

Because power equipment is exposed to distinct voltage levels, semiconductors with different voltage characteristics must be used.

Reference [13] proposes a new approach to combine IGBT fast frequency switching capability with a high voltage blocking capability in some semi-conductor devices such as GTO transistors. This equipment is modulated differently. As a result, high-voltage cells operate at low frequencies, and low-voltage cells operate at high

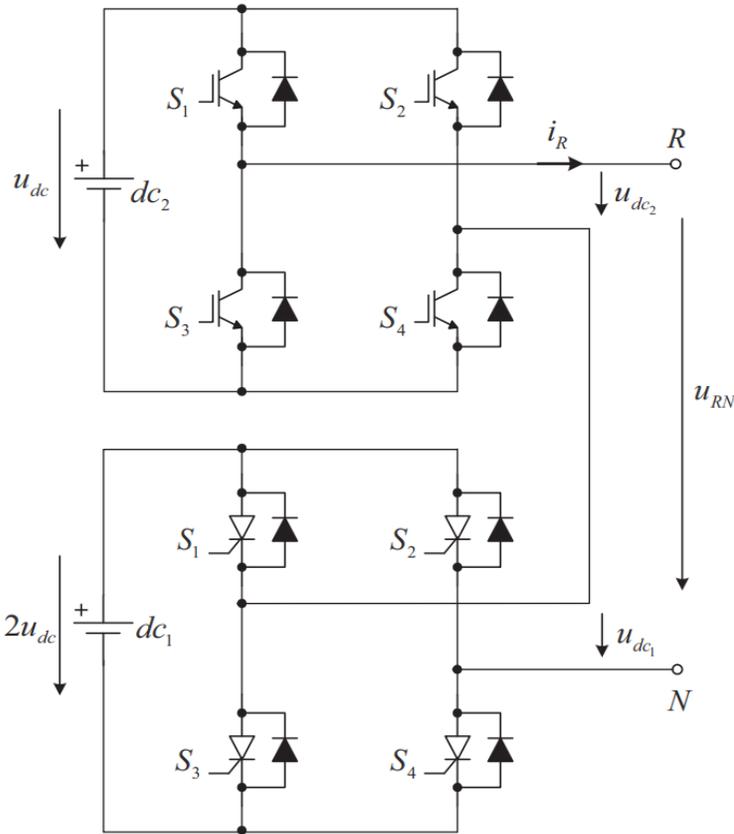


Figure 1.10 Single-phase asymmetric hybrid cascaded H-bridge IGBT and GTO

frequencies. The theory of combining the advantages of different semi-conductors has also been extended to the field of topologies. Different structures are combined to create a multi-level inverter and to integrate the quality and strengths of each topology. Reference [13] has replaced high-voltage three-phase cells with NPC clamp inverters

to reduce the number of isolated dc sources. This reference uses six-switch two-level inverters (instead of high-voltage single-phase cells) to investigate the even number of output voltage levels [15]. Recently, a new approach based on the combination of NPCs and floating capacitor inverters has been introduced by Barbosa [19].

1.5.1 Distinct semi-conductors

Asymmetric topologies increase the number of output voltage levels. This is accomplished with isolated dc sources with distinct voltage levels. The importance of a power component in this structure is proportional to the voltage level used. Therefore, the equipment in high voltage cells should be able to block higher voltages compared to low voltage cells. This feature provides a degree of freedom in the use of semiconductors and allows them to take advantage of their advantages and strengths. In addition, recent studies in the field of semiconductor technologies describe how power equipment is selected in terms such as switching frequency and voltage blocking capability. Semi-conductors with this capability, such as GTO transistors, usually have a limited switching speed. Also, faster equipment such as IGBT isolated gate bipolar transistors are capable of blocking the maximum voltage to take advantage of asymmetric cascaded H-bridge inverters and the advantages of seven-level hybrid cascaded topology semiconductor equipment as shown in Figure 1.10 in [13].

To ensure proper system operation, a new modulation strategy is required, in which the GTO inverter is modulated so that it is switched only at the main frequency, and the IGBT inverter is used so that it is switched only at the higher frequency.

1.5.2 Three-phase cascaded NPC and single-phase H-bridge

Hybrid inverters do include not only different semiconductor devices but also use distinct topologies to overcome the limitations of existing structures. One of the biggest disadvantages of a cascaded H-bridge inverter is a large number of dc sources required. The most commonly used solution is to use asymmetric dc sources. In some users, the number of remaining dc resources may limit the use of this topology. To

reduce the number of dc sources required, Steamer and Monger-Ker introduced a hybrid multi-level cascaded inverter. This design combines a three-phase NPC inverter with a single-phase H-bridge inverter, as shown in Figure 1.11.

The number of voltage levels generated by the NPC inverter is equal to the single-phase H-bridge topology. The use of common interface circuits for all three phases is the most important advantage of this design. This advantage leads to a reduction of dc sources from 6 to 4 and is reflected in the asymmetric nine-level cascaded inverter in Figure 1.11. The dc-link voltages of an asymmetric hybrid inverter are formed in a ratio of 3:1 and produce a 9-level voltage at the output. The NPC inverter uses voltage-blocking IGBTs to generate active power with fewer losses. IGBT fast switching capability is also used for single-phase H-bridge inverters and harmonic output reduction.

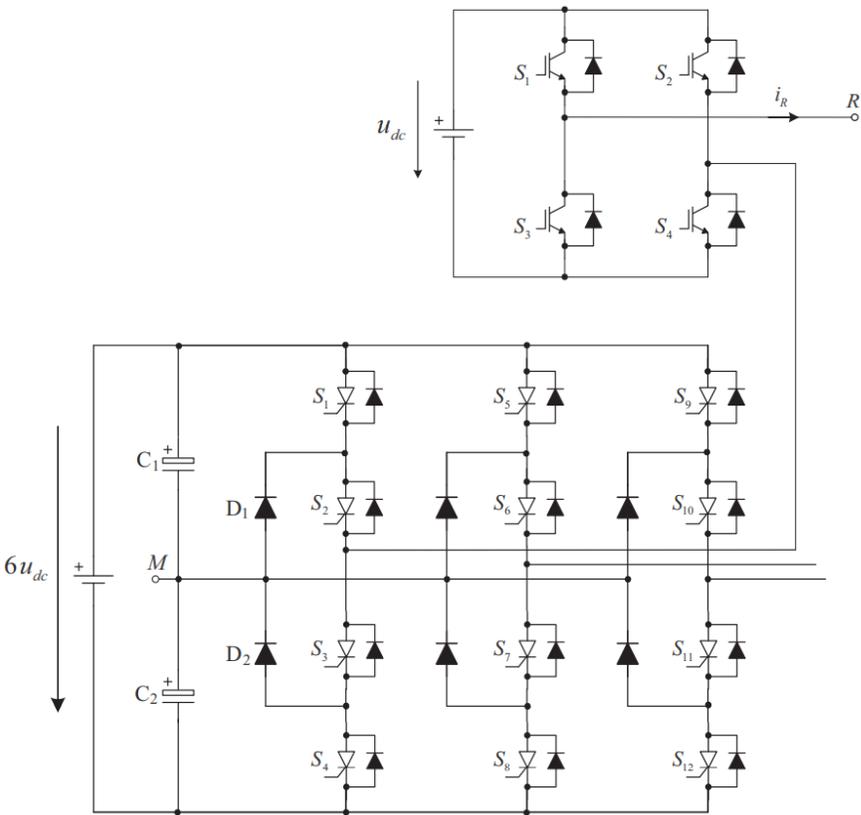


Figure 1.11 Asymmetric hybrid multi-level inverter with three-phase NPC and single-phase H-bridge

1.5.3 Three-phase cascaded H-bridge and single-phase H-bridge

The number of output voltage levels generated by symmetric or asymmetric cascaded inverters is limited to odd numbers. In some specific applications, the number of voltage levels generated at the output is an even number to achieve optimum power. In some scenarios, a three-level method would be inadequate; however, a five-level inverter would result in component complexity. Therefore, a four-level inverter is the most optimal approach. To achieve the number of even output voltage levels while maintaining the intrinsic advantages of the cascade inverter, a series connection between the three-phase six-switch inverter and the single-phase H-bridge is essential, as reflected in Figures 1.12 in papers [15-16]. This approach also makes it possible to reduce the number of dc sources required compared to the cascaded structure.

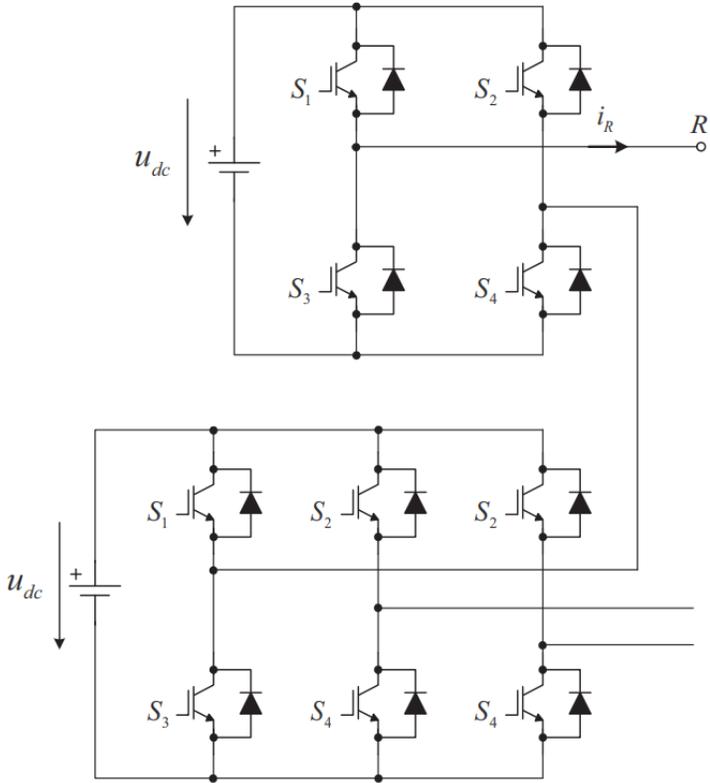


Figure 1.12 Asymmetric hybrid multi-level inverter with three-phase H-bridge and single-phase H-bridge

1.5.4 ANPC Inverter

A hybrid symmetric multi-level inverter with slight differences has been proposed by Barbosa [19]. This inverter combines the flexibility of a multi-level floating capacitor inverter with the capabilities of an NPC inverter and generates multi-level voltages. In addition, it uses a dc-link source on the NPC and controls the voltage of the floating capacitors with the existing switching states.

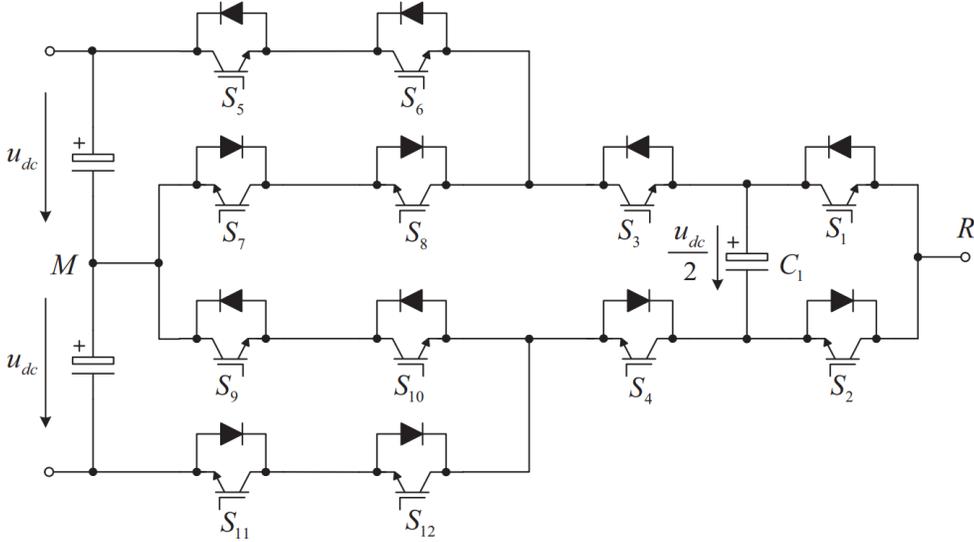


Figure 1.13 Five-level ANPC

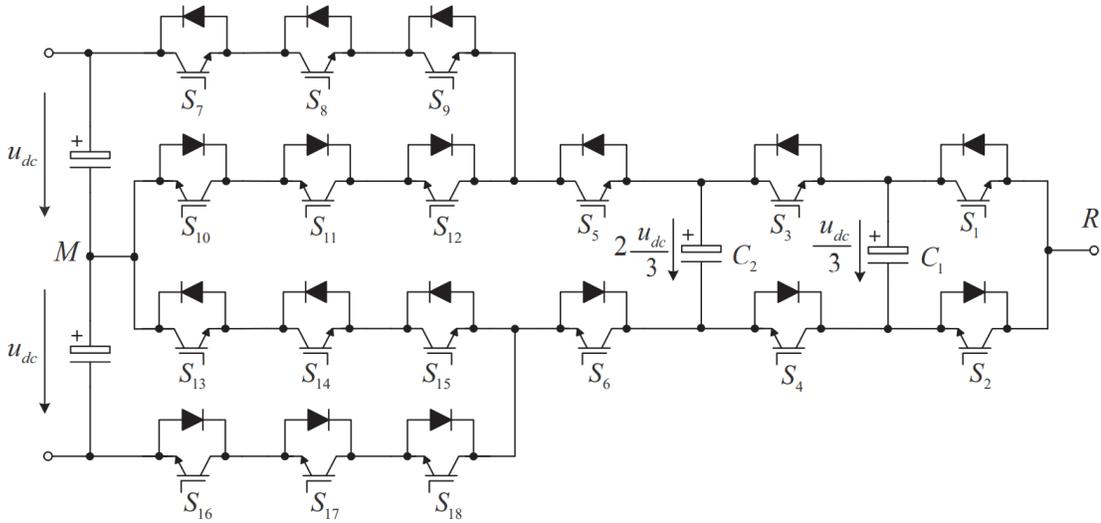


Figure 1.14 Seven-level ANPC

Hence the advantage of the cascaded approach is the use of multiple dc sources, as shown in Figure 1.13. An S_5 and S_6 series connection is required to keep the voltage constant at $U_{DC}/2$ for all switches. It can be changed by adding series switches and increasing the number of cascaded two-level inverters, which is shown for a seven-level structure in Figure 1.14.

1.6 Comparison of topologies

The choice of multi-level topology is related to the applications and specifications required, such as power losses, cost and area. The number of components plays an important role. For guidance in selecting the appropriate multi-level topology, Tables 1.9 show the number of semiconductors and components required by different topologies. In this analysis, multi-level asymmetric cascades, three-phase cascaded NPCs and single-phase cascaded H-bridges are not considered, as they are used for applications with more than seven levels $m \geq 7$. Analyses show that the same number of switches (12) are required to achieve three-level voltage in NPCs and FCs and symmetric cascaded H-bridge inverters. Although the number of dc sources and the required elements are different, the advantage of FC and NPC topologies over the cascaded H-bridge system is that an integrated transformer is required to supply independent and different dc sources. If multiple dc sources are available, the cascaded H-bridge topologies are the most sensible solution, as they require fewer components. Increasing the number of clamp components increases the balance of rotating capacitors and dc-link and limits the use of FC and NPC inverters for applications with more than three levels. In the five-level approach, the number of switches used by the ANPC inverter is very large, but the ANPC inverter seems to be a good choice because it does not require a clamp diode and uses only three floating capacitors. In addition, the dc-link is split between the two capacitors reducing the balance complexity.

Table 1.9 Comparison of multi-level inverters based on the number of components and isolated source

Structure	Levels	Switches	Diodes (Clamping)	Capacitors (Floating)	Capacitor (dc-Link)	dc- Sources
NPC	3	12	6	0	2	1
	5	24	36	0	4	1
	m	6(m-1)	3(m-1)(m-2)	0	m-1	1
FC	3	12	0	3	2	1
	5	24	0	18	4	1
	m	6(m-1)	0	3/2(m-1)(m-2)	m-1	1
SCH-B	3	12	0	0	3	3
	5	24	0	0	6	6
	m	6(m-1)	0	0	3/2(m-1)	3/2(m-1)
Active NPC	3	12	-	-	-	-
	5	24	0	3	2	1
	m	9(m-1)	0	3/2(m-3)	2	1

1.7 Conclusion

After the introduction of the NPC three-level inverter, the use of multi-level inverters has expanded due to the ability to use more than two voltage levels to supply a sinusoidal output voltage. Multi-level inverters provide quality improvement conditions, the possibility of using low voltage power equipment, reducing switching losses and reducing the effects of electromagnetic interference. One of the introduced multi-level topologies is the structure of FC and NPC, which works based on the concept of voltage blocking in power switches through diodes and capacitors. These concepts are widely used in industry, but the requirement to connect the elements in series limits the practical applications of this technology. In recent years, the method of using clamp components has emerged. A Cascaded H-bridge inverter produces

multi-level output voltage by connecting a series of single-phase H-bridge inverters. Each phase requires an isolated dc source. This has limited the use of these topologies in specific applications. Special strategies have been introduced to overcome this limitation. If an asymmetric cascaded H-bridge uses dc sources with different values, it can produce a large number of levels. This feature creates a degree of freedom in using cells with different voltage rates and semiconductors with different voltage blocking capabilities. This principle emphasizes the combination of semi-conductors with diverse specifications and creates a new group of multi-level topologies called hybrid multi-level inverters. This approach provides the advantages and strengths of different topologies by combining them with multi-level structures. Although most multi-level topologies have a different circuit structure, they all have good control over dc-link capacitors and floating capacitors. To assist designers in choosing the right topology for your inverter, this chapter compares multi-level topologies with criteria such as the number of isolated dc source components. It is important to note that in three-level topologies, NPCs, FC inverters, and cascaded H-bridge inverters have the same number of switches, but the blocking elements and the number of dc sources required are different. One of the disadvantages of the cascaded method is the need for two isolated dc sources, while the NPC and FC topologies require only one source. The big challenge of FC inverters is the need for a special control strategy for capacitors. FC and NPC are rarely used for five-level topologies because they require large clamping components. In single dc source applications, ANPC seems to be a good solution, as it uses only three floating capacitors, and the dc-link is provided by two capacitors. This design reduces the complexity of balance. Based on these analyzes, it was determined that three-level NPC and five-level ANPC would be used.

Chapter 2

Literature Review of The Impedance Source Converters

2.1 Introduction

Network-connected converters need to increase the voltage in the power electronics field due to limited (dc) supplies. Traditional converters, such as voltage source converters, have a step-down property and consequently require more dc-dc converters to increase the voltage. This increases the cost and reduces the efficiency of the entire system. The advent of impedance source converters [1] has reduced the limitations and received much attention. Today, these converters are used in applications such as motor drives [2,3], photovoltaic systems [4,5], fuel cells [6], distributed power sources [7] and uninterruptible power supplies [8]. In this chapter, we first introduce traditional converters; then discuss the details of impedance source converters.

2.2 Traditional converters

2.2.1 Voltage Source Converter (VSC)

Figure 2.1 shows a voltage source converter in which a dc voltage source supplies the main circuit. The dc voltage source may be a capacitor, battery or fuel cell. Six switches are used in the main circuit consisting of a transistor and a parallel diode in the opposite direction. Voltage source converters have a variety of applications in the industry but suffer from the following limitations:

- a. The alternating output (ac) voltage is less than the direct current (dc) input voltage, so voltage source converters act as a reducing inverter or increasing rectifier. The increase in voltage is provided by adding a boost circuit (dc to dc). Adding this extra equipment increases cost and reduces efficiency.
- b. Simultaneous switching on the upper and lower switches of each phase leads to a short circuit and damage the circuit components. Therefore, a dead time is applied to prevent this phenomenon, which in turn causes distortion of the waveform and the formation of harmonics.

c. Using the passive filter to sine the output waveform and reduce the harmonic voltage causes additional control and more power losses [1].

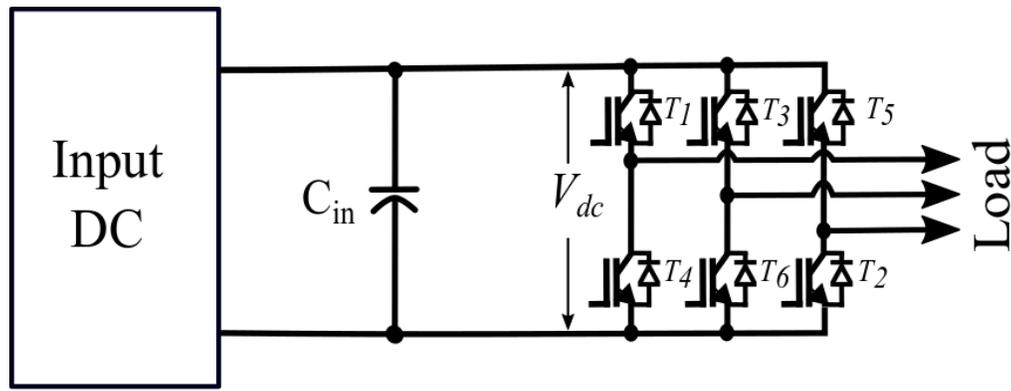


Figure 2.1: Voltage source Inverter (VSI)

2.2.2 Current Source Converter (CSC)

Figure 2.2 shows a three-phase current source converter to power a direct current (dc) source in the main circuit. The direct current source can be a relatively large inductor powered by a battery, fuel cell, or diode rectifier. Six switches are installed in the main circuit consisting of power semiconductors (GTO and a power transistor with a series diode to supply DC) with the tolerance ability tolerate reverse voltage. At the same time, current source converters suffer from the following limitations:

- a. The output ac voltage in this converter is always higher than the input voltage (dc). Therefore, the current source converter is a step-up inverter or a step-down rectifier. To reduce the output voltage, a buck converter is applied and, like the voltage source converter, will increase losses and control complexity.
- b. At any point in time, at least one of them up or down switches must be on to prevent the danger of an open inductor current circuit. Therefore, it is necessary to consider an overlap time of a few microseconds. This process distorts the output waveform and creates a harmonic.

c. Switches must be capable of withstanding reverse voltage. This is realized by connecting a series of diodes with fast transistors or IGBT [1].

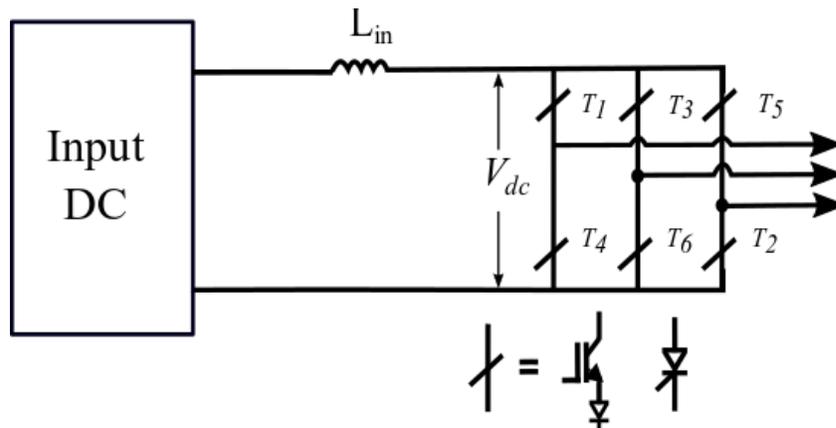


Figure 2.2: Current source inverter (VSI)

Voltage source and current source converters suffer from the following disadvantages:

- a. These converters do not have the ability to increase or decrease voltage simultaneously.
- b. These converters cannot be connected to each other. That is, a current converter cannot be used instead of a voltage converter, and vice versa.
- c. Both converters are vulnerable to electromagnetic interference

2.3 Impedance source converters

In order to overcome the limitations of traditional converters, in 2003, impedance source converters called Z-Source Converters (ZSC) were introduced by Professor Peng et al. These converters have the ability to transfer power in all states (ac to dc, dc to ac, dc to dc, ac to ac). Figure 2.3 reflects the overall structure of an impedance source converter.

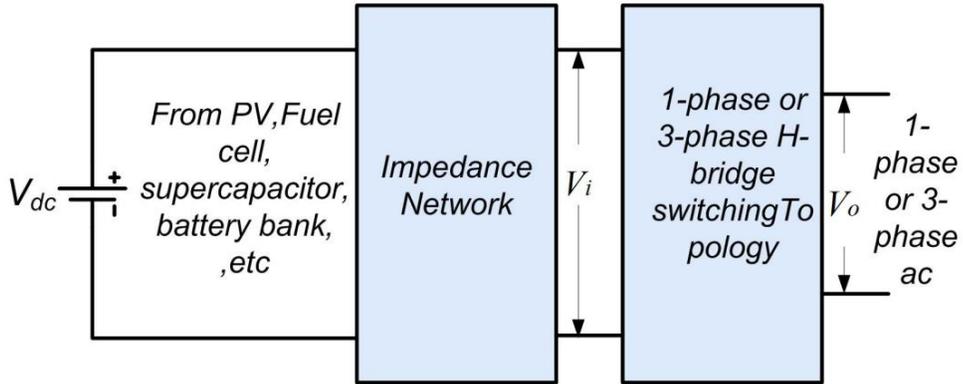


Figure 2.3: The general structure of the impedance source converter [1].

This converter consists of three main parts, including a power supply, impedance network and main circuit. The most important difference with a traditional converter is the structure of the impedance network. The impedance network of this converter consists of two inductors and two capacitors connected to each other in the form of X. This set acts as a second-order filter and eliminates output voltage distortions, and is much more efficient than the capacitor used in the voltage source converter. The inductor used in the impedance network also drastically reduces the push current and current harmonics [10].

The power supply can be a current source or a voltage source. Therefore, the dc power supply can be a battery, a capacitor, a diode rectifier, an inductor or a combination of these components.

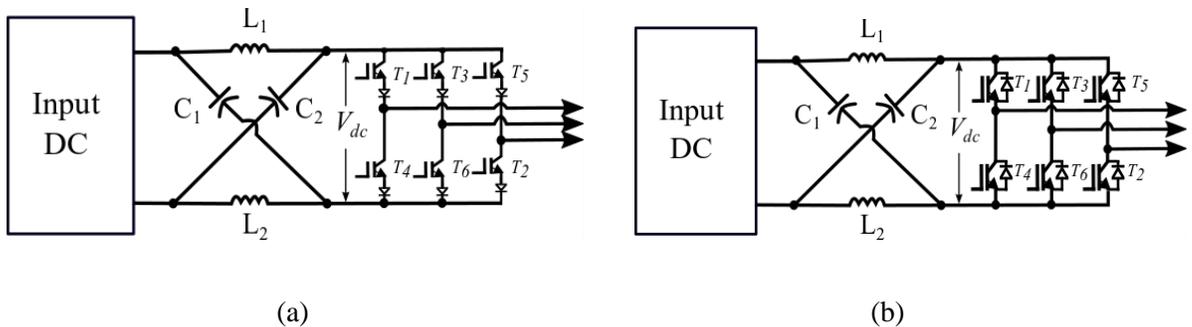


Figure 2.4: Impedance source converter: (a) Parallel reverse, (b) Switch and diode connected in series [1].

The switches used in this converter can be a parallel reverse combination, including a switch and a diode. Figure 2.4 shows two three-phase impedance source converter structures with different switches. In theory, using an impedance source inverter leads to a voltage from zero to infinity. In fact, this converter, unlike traditional converters, can work like a high-spectrum buck-boost circuit.

In [6] and [11], the required components of voltage source inverters, voltage source with a boost converter an impedance source with the power of 50 kW and input voltage in the range of 250 to 420 volts are compared. A summary of this comparison process is shown in Table 2.1.

Table 2.1 Components required for three different inverters

<i>Inverter</i>	Number of inductors	Inductance μH	Average current of inductors	Number of capacitors	Capacity of capacitors μF	Capacitors voltage range	Number of diodes
<i>Voltage source</i>	0	-	-	1	667	420	1
<i>Voltage source with boost converter</i>	1	510	200	1	566	420	2
<i>impedance source</i>	2	339	200	2	405	420	1

The following section discusses recent developments in impedance source converters (abbreviated as Z-source). The governing relationships of each topology are extracted. As introduced in the first part of chapter 2, the impedance source converter can transfer power in all states, but only the inverter state (DC to AC) has been investigated in this chapter.

2.3.1 Z-Source Inverter (ZSI)

Z-Source Inverter (ZSI) topology is a base topology for other impedance source inverters. This is shown in figure 2.5. The relationships of this topology are fully proven.

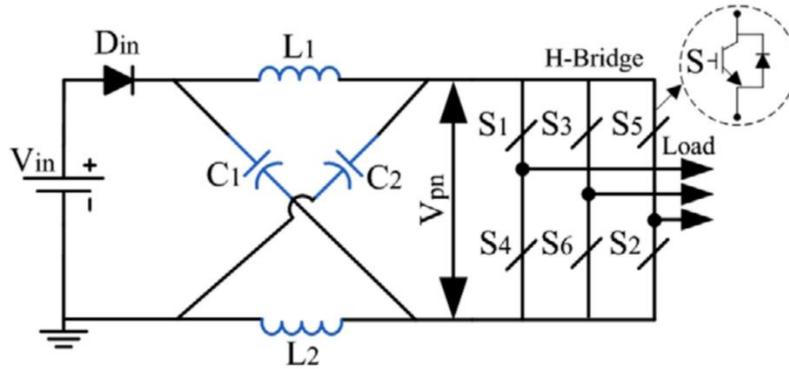


Figure 2.5: Basic topology of Z-Source inverter [1].

To prove the relationships, the topology of the converter is evaluated in two active and short circuit states. Figure 3.6 shows the circuit corresponding to the active state (shot through) and the short circuit (Non shot through) state.

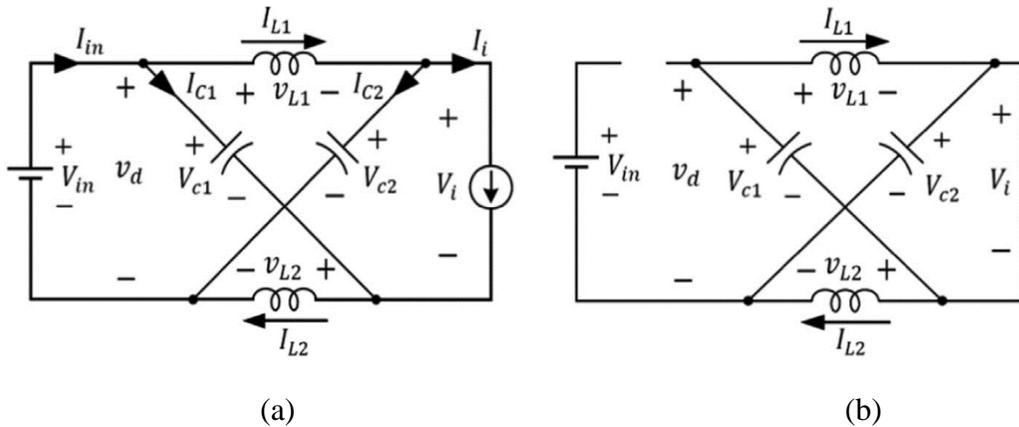


Figure 2.6: States of circuit: (a) active state, (b) short circuit.

Assume that the values L_1 and L_2 the values C_1 and C_2 are equal and equivalent to L and C , respectively. In this case, the circuit becomes a symmetric circuit. As a result, we have:

$$V_{C1} = V_{C2} = V_C, \quad v_{L1} = v_{L2} = v_L \quad (2.1)$$

If a short circuit occurs during the time T_0 of the entire switching cycle T , the diode converts to reverse bias, and no voltage is generated at the dc-link (Figure 3.6b). As a result, we have:

$$v_L = V_C, \quad v_d = 2V_C, \quad v_i = 0 \quad (2.2)$$

If during time T_1 of the entire switching cycle T , the inverter bridge is in one of eight active states (Figure 3.6a); as a result, we have:

$$v_L = V_0 - V_C, \quad v_d = V_0, \quad v_i = V_C - v_L = 2V_C - V_0 \quad (2.3)$$

The average voltage of the two ends of the inductor in a switching cycle is zero, so concerning the relations (3.2) and (3.3), we have:

$$V_L = \bar{v}_L = \frac{T_0 \cdot V_C + T_1 \cdot (V_0 - V_C)}{T} = 0 \quad (2.4)$$

where $T = T_1 - T_0$. Summarizing the above relation leads to the following relation:

$$\frac{V_C}{V_0} = \frac{T_1}{T_1 - T_0} \quad (2.5)$$

Similar to inductor voltage, the average voltage between the two ends of the inverter bridge in the switching cycle is zero, so we have:

$$V_L = \bar{v}_i = \frac{T_0 \cdot 0 + T_1 \cdot (2V_C - V_0)}{T} = \frac{T_1}{T_1 - T_0} V_0 = V_C \quad (2.6)$$

By placing the relation (2.6) in the relation (2.3), we have:

$$\bar{v}_i = V_C - v_L = 2V_C - V_0 = \frac{T_1}{T_1 - T_0} V_0 = B \cdot V_0 \quad (2.7)$$

where B indicates the inverter boost factor and is calculated as follows.

$$B = \frac{T}{T_1 - T_0} = \frac{1}{1 - 2\frac{T_0}{T}} \geq 1 \quad (2.8)$$

The peak output voltage \hat{v}_{ac} according to Equation (9) depends on the peak voltage of the dc link (\bar{v}_i).

$$\hat{v}_{ac} = M \cdot \frac{\hat{v}_i}{2} \quad (2.9)$$

Placing the relation (2.7) in (2.9) leads to:

$$\hat{v}_{ac} = M \cdot B \cdot \frac{\hat{v}_i}{2} = G \cdot \frac{V_0}{2} \quad (2.10)$$

where the G is the buck-boost factor of the inverter, and its value varies between 1 to infinity. Based on the relations (2.2), (2.6) and (2.8), the voltage of the capacitors is expressed as follows.

$$V_{C1} = V_{C2} = V_C = \frac{1 - \frac{T_0}{T}}{1 - 2\frac{T_0}{T}} V_0 = \frac{1 - D}{1 - 2D} v_0 \quad (2.11)$$

Z-Source Inverter is the first type of impedance source converter that suffers from the following disadvantages:

1. Its boosting factor is not very high.

2. The only way to increase the boost factor is to increase D (or decrease M). To achieve a high boost factor, the value of M must be reduced, which in turn causes distortion in the output waveform and increases the voltage stress of the components.
3. Its input current is discontinuous.

2.3.2 Quasi Z-Source Inverter (qZSI)

The general topology of the Quasi Z-Source inverter is shown in Figure 2.7. The number of components in its topology is the same as Z-Source Inverter. However, the connection of components in its impedance network is such that this topology has a continuous input current and lower voltage stress than traditional converters [15].

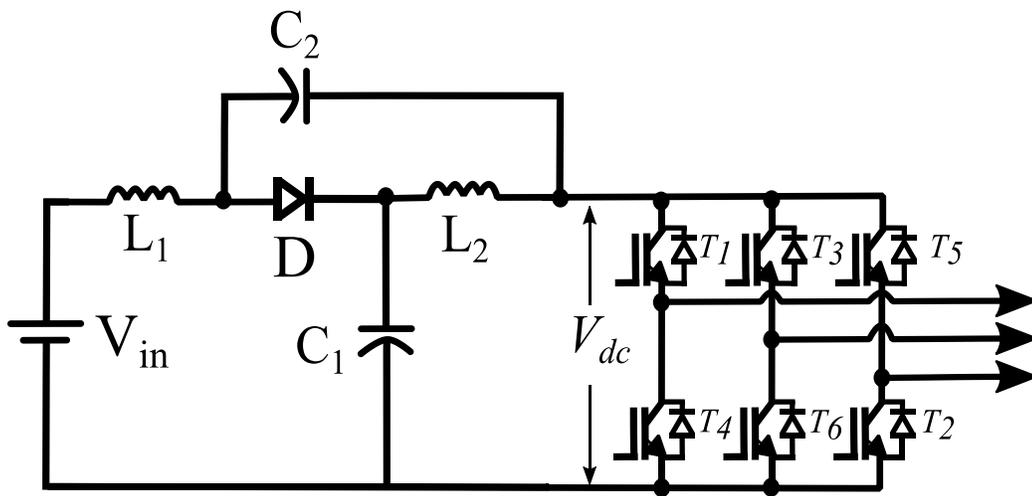


Figure 2.7: Quasi Z-Source Inverter.

All relations of this converter are similar to the impedance source converter (except capacitor voltage C_2) and are expressed as follows:

$$V_{C1} = \frac{1 - D}{1 - 2D} V_{in} \quad (2.12)$$

$$V_{C2} = \frac{D}{1 - 2D} V_{in} \quad (2.13)$$

$$B = \frac{1}{1 - 2D} \quad (2.14)$$

$$\hat{v}_{ac} = \frac{1}{1 - 2D} \left(\frac{MV_{in}}{2} \right) \quad (2.15)$$

2.3.3 Improved Z-Source Inverters (I-ZSI)

Figure 3.8 shows the overall topology of this inverter. As shown in the figure, this topology is the same as the Z-Source inverter regarding the number of components. But the connection method and connection position of the two impedance networks are different. This slight change reduces the stress on the capacitor voltage and limits the surge current at the start [16]. Also, the boost factor and control method of this converter are the same as the Z-Source inverter.

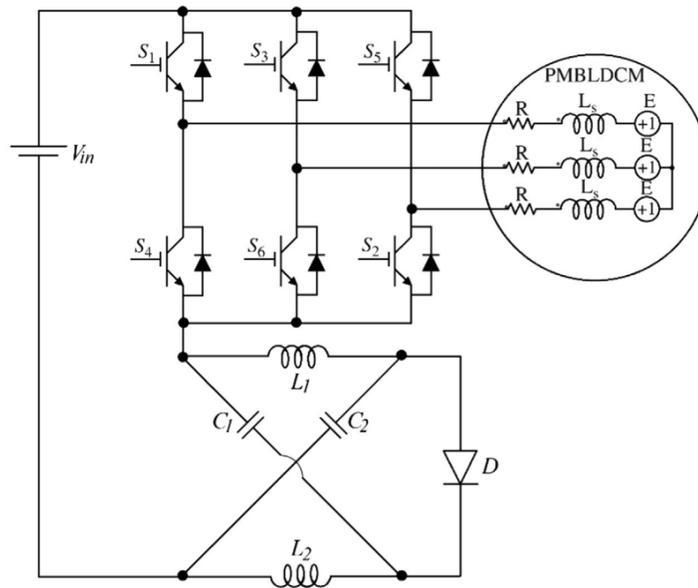


Figure 2.8: Improved Z-Source Inverter.

Figure 2.9 compares the stress curve of the capacitor voltage V_C/V_0 based on the switching cycle ratio D_0 for Z-Source Inverter and Improved Z-Source Inverter converters. As it turns out, the voltage stress on the capacitors in the Improved Z-Source Inverter is less.

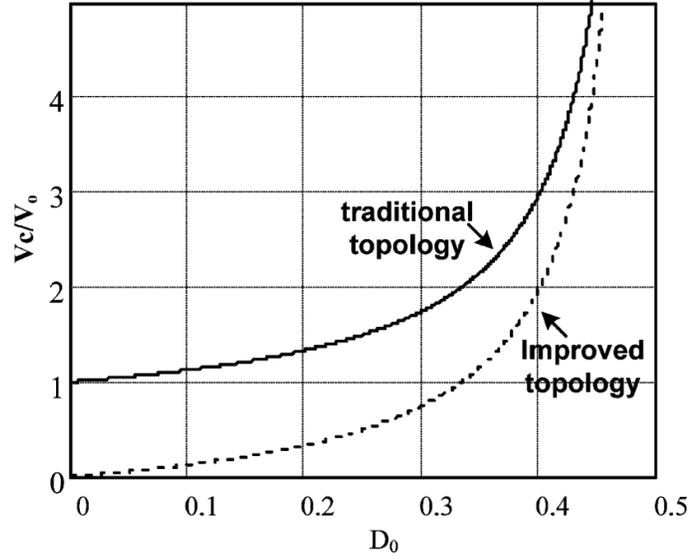


Figure 2.9: Comparison of voltage stress of capacitor in Z-Source Inverter and Improved Z-Source Inverter converters [16].

Important relationships in this converter are:

$$\hat{v}_{PN} = BV_0 = \frac{1}{1 - 2D_0} V_0 \quad (2.16)$$

$$V_{C1} = V_{C2} = V_C = \frac{D_0}{1 - 2D_0} V_0 \quad (2.17)$$

The capacitor voltage depends on the switching cycle, as stated in Equation (2.17), so a gradual increase D_0 from zero to a certain value gradually increases the capacitor voltage from zero to the desired value. Controlling parameter D_0 in the converter softly limits the surge current. This feature is not available in traditional impedance source converters. Capacitor voltage ripple and inductor current ripple in this converter are based on Equations (2.18) (2.19).

$$\Delta V_C = \frac{I_L D_0 T}{C} \quad (2.18)$$

$$\Delta i_L = \frac{D_0 TV_C}{L} = \frac{D_0(1 - D_0)TV_0}{(1 - 2D_0)L} \quad (2.19)$$

In the above relations, I_L , C and L are equal to the average inductor current, capacitor capacity and inductor inductance, respectively.

2.3.4 Switched Inductor Z-Source Inverters (SL-ZSI)

The general topology of this converter is shown in Figure 2.10. As shown in the figure, this converter is similar to the traditional Z-Source Inverter. Instead of impedance network inductors, switched inductor cells (consisting of two inductors and three diodes) are used [17]. In the short circuit and active state, the inductors of each cell have parallel and series connections, respectively. The boost factor of this converter is higher than the traditional converter, but it faces problems such as discontinuity of the input current, the surge current at the moment of the start, and so on.

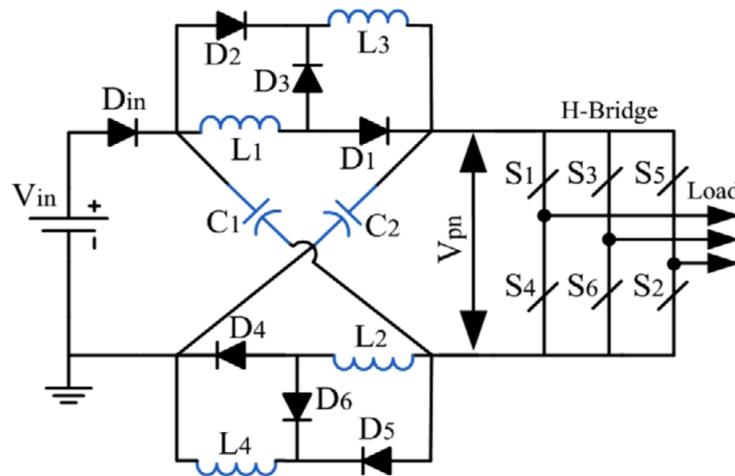


Figure 2.10: Switched Inductor Z-Source Inverter.

Boost factor, capacitors voltage and voltage gain of this converter are extracted using the following relations:

$$B = \frac{1 + D}{1 - 3D} = \frac{1 + (T_0/T)}{1 - 3(T_0/T)} \quad (2.20)$$

$$V_{C1} = V_{C2} = V_c = \frac{1 - D}{1 - 3D} V_{in} \quad (2.21)$$

$$G_{max} = MB_{D-1-M} = \frac{M(2 - M)}{3M - 2} \geq G_{0-s} \quad (2.22)$$

$$G_{0-s} = \frac{M}{2M - 1} \quad (2.23)$$

In Equation 2.22, inverter voltage gain calculated is smaller than the voltage gain of the converter. Based on this equation, the voltage stress of the capacitors in this converter with the same D is more than the traditional converter.

2.3.5 Switched Inductor Quasi Z-Source Inverter (SL-qZSI)

The topology of a Switched Inductor Quasi Z-Source Inverter is shown in Figure 2.11. As can be seen in the figure, the topology of this converter is similar to the Quasi Z-Source Inverter, but instead of one of the inductors, a switching inductor cell is installed.

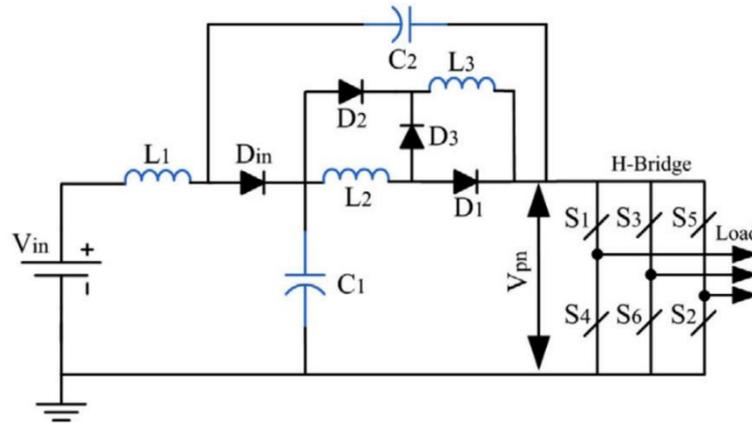


Figure 2.11: Switched Inductor Quasi Z-Source Inverter.

This converter has all the advantages of previous converters, such as input current continuity and reduction of inrush current at the moment of start. In addition, it has a higher boost factor than the Quasi Z-Source Inverter. Another advantage of this converter is reducing the number of passive components [18]. The boost factor and the voltage of the capacitors in this converter are obtained based on the relations (2.24) (2.25), respectively.

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1 + D}{1 - 2D - D^2} \quad (2.24)$$

$$\begin{cases} V_{C1} = \frac{1 - D}{1 - 2D - D^2} V_{dc} \\ V_{C2} = \frac{1 - D}{1 - 2D - D^2} V_{dc} \end{cases} \quad (2.25)$$

The control method of this converter is the maximum boost method, so by inserting Equation (2.6) in Equation (2.24), we have:

$$B = \frac{1 + \bar{D}}{1 - 2\bar{D} - \bar{D}^2} = \frac{8\pi^2 - 6\sqrt{3\pi} \cdot M}{-8\pi^2 + 24\sqrt{3\pi} \cdot M - 27M^2} \quad (2.26)$$

At present, the voltages gain (G) and the peak voltages of the output phase \hat{v}_{ph} are obtained based on the modulation index:

$$G = MB = \frac{8\pi^2 M - 6\sqrt{3\pi} \cdot M^2}{-8\pi^2 + 24\sqrt{3\pi} \cdot M - 27M^2} \quad (2.27)$$

$$\hat{v}_{ph} = \frac{MV_{PN}}{2} = \frac{MBV_{dc}}{2} \quad (2.28)$$

2.3.6 Trans Z-Source Inverter (T-ZSI)

The general topology of the Trans Z-Source Inverter is shown in Figure 2.12. In converters containing transformers, changing the conversion ratio of the transformer leads to changing the boosting factor. The only way to change the boost factor in some converters is to change the switching cycle ratio (D). Of course, this method is not very effective due to power quality limitations [19]. An important drawback of this converter is its use in applications that require high boosting. Because increasing the cycle ratio increases the volume, cost and power losses [21].

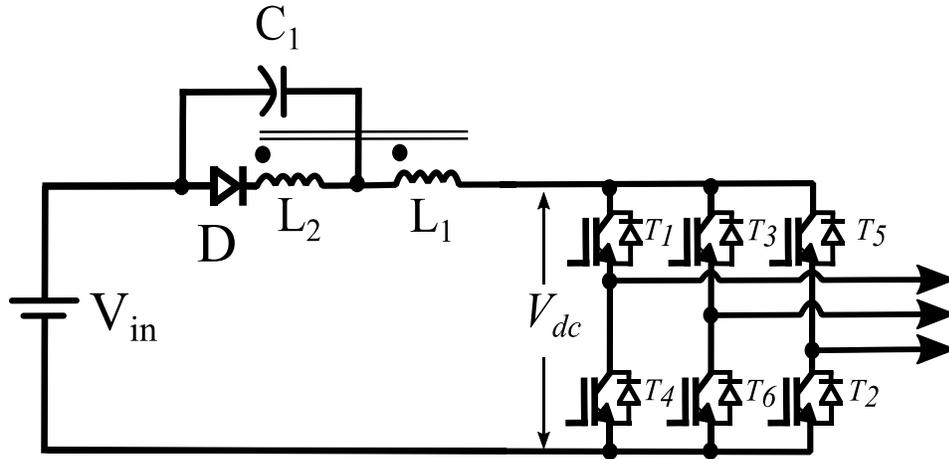


Figure 2.12: Trans Quasi Z-Source Inverter

Boost factor and capacitor voltage in this converter are calculated based on the following equations:

$$B = \frac{\hat{v}_i}{V_{dc}} = \frac{1}{1 - (1 + n)D} \quad (2.29)$$

$$V_{C1} = \frac{n \cdot D}{1 - (1 + n)D} V_{dc} \quad (2.30)$$

In the above relations, $n = \frac{N_2}{N_1}$ indicates the conversion ratio of the transformer. The control method used in this converter is the maximum fixed boost, so by embedding the relation (2.9) in (2.29), we have:

$$B = \frac{\hat{v}_i}{V_{dc}} = \frac{1}{1 - (1 + n) \left(1 - \frac{\sqrt{3}}{2} M\right)} \quad (2.31)$$

According to the relation (2.31), the voltage gain is calculated in the modulation index.

$$G = MB = \frac{M}{1 - (1 + n) \left(1 - \frac{\sqrt{3}}{2} M\right)} \quad (2.32)$$

2.3.7 Improved Trans Z-Source Inverter (IT-ZSI)

The general topology of this converter is shown in Figure 2.13. The topology of this converter is similar to the Z-Source Inverter, but instead of one of the inductors, a transformer with a conversion ratio of $n:1$ is used. The advantages of this converter are:

- High boosting factor
- Continuous input current
- Reduce current resonance at the start

Compared to the Trans Z-Source Inverter and the Trans Quasi Z-Source Inverter, this converter has a higher modulation index, which reduces the component voltage stress and reduces the input current ripple. Also, if the constant modulation index is set for the same inputs and outputs, this converter requires a smaller conversion ratio than the other two converters [20].

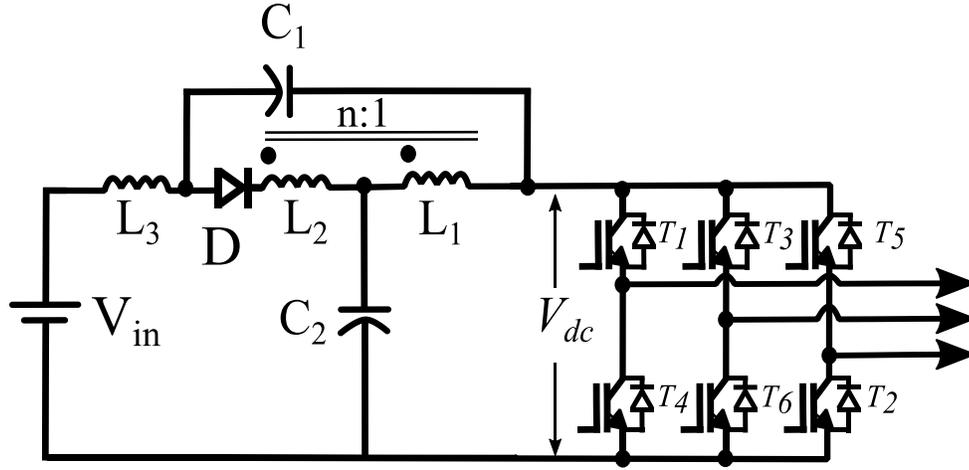


Figure 2.13: General topology of Improved Trans Z-Source Inverter [20].

The relations obtained from the analysis of this converter are as follows.

$$\begin{cases} V_{C1} = \frac{1-D}{1-(2+n)D} V_{dc} \\ V_{C2} = \frac{(1+n)D}{1-(2+n)D} V_{dc} \end{cases} \quad (2.33)$$

$$V_{PN} = \frac{1}{1-(2+n)D} V_{dc} = BV_{dc} \quad (2.34)$$

$$B = \frac{1}{1-(2+n)D} = \frac{1}{1-(2+n)\frac{T_0}{T}} \quad (2.35)$$

$$\hat{v}_{ph} = M.B. \frac{V_{dc}}{2} \quad (2.36)$$

Where $n = \frac{N_2}{N_1}$ is the conversion ratio of the transformer. The control method used in this converter is the fixed maximum boost method, so by embedding the relation (2.9) in (2.5), we have:

$$B = \frac{1}{1-(2+n)\left(1 - \frac{\sqrt{3}}{2}M/2\right)} \quad (2.37)$$

Based on the equation (2.37), we can calculate the voltage gain in terms of the modulation index.

$$G = \frac{\hat{v}_{ph}}{\frac{V_{dc}}{2}} = M.B = \frac{M}{1 - (2 + n) \left(1 - \frac{\sqrt{3}}{2} M/2\right)} \quad (2.38)$$

2.3.8 Sigma Z-Source Inverters (Sigma-ZSI)

Sigma Z-Source Inverter is in the class of transformer-based converters. As shown in the figure, this converter has two transformers and two capacitors in its impedance network, which are cross-connected. The impedance network of this converter contains two gamma mirror networks. The disadvantage of transformer-based converters such as Trans Z-Source Inverter, Gamma, Y, etc., is that increasing the converter boost factor requires increasing the transformer cycle. This leads to an increase in transformer volume in applications requiring a high voltage gain. The Sigma converter achieves the highest gain with a cycle ratio of less than 1.618 [21].

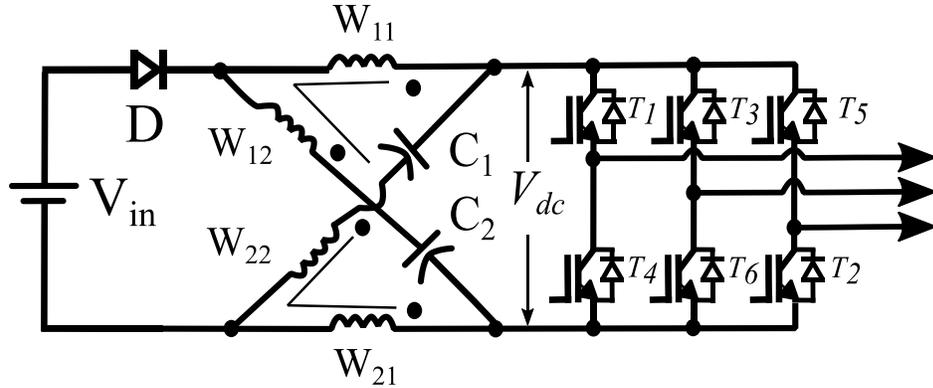


Figure 2.14: Sigma Z-Source Inverters [21].

$$V_{C1} = V_{C2} = V_C = \frac{(1 - D_0)}{1 - (2 + \left(\frac{1}{n_{r1} - 1}\right) + \left(\frac{1}{n_{r2} - 1}\right))D_0} V_{dc} \quad (2.39)$$

$$B = \frac{1}{1 - (2 + \left(\frac{1}{n_{r1} - 1}\right) + \left(\frac{1}{n_{r2} - 1}\right))D_0} V_{dc} \quad (2.40)$$

The following equation shows the voltage gain ratio of a traditional Z-Source Inverter and a Sigma Z-Source Inverter.

$$\frac{G_{\epsilon ZSI}}{G_{ZSI}} = \frac{MB_{\epsilon ZSI}}{MB_{ZSI}} = \frac{1 - 2(1 - M)}{1 - (2 + (\frac{1}{n_{r1}} - 1) + (\frac{1}{n_{r2}} - 1))(1 - M)} \quad (2.41)$$

In the relations (2.39) to (2.41), $n_{r1} = W_{11}/W_{12}$ and $n_{r2} = W_{21}/W_{22}$ the conversion ratios of the transformers are high and low, respectively.

2.3.9 L-Z-Source Inverter (L-ZSI)

As shown in Figure 2.15, the impedance network topology of this converter, unlike other Z-Source Inverters, consists only of inductors and diodes. The lack of capacitors in the impedance network solves the moment of start problems. Features of this converter are:

- Common ground between the power supply and the main circuit
- Input current continuity
- Setting the boost factor by increasing the number of inductors and setting the switching cycle ratio [22]

Disadvantage of this converter is:

- Low boost factor

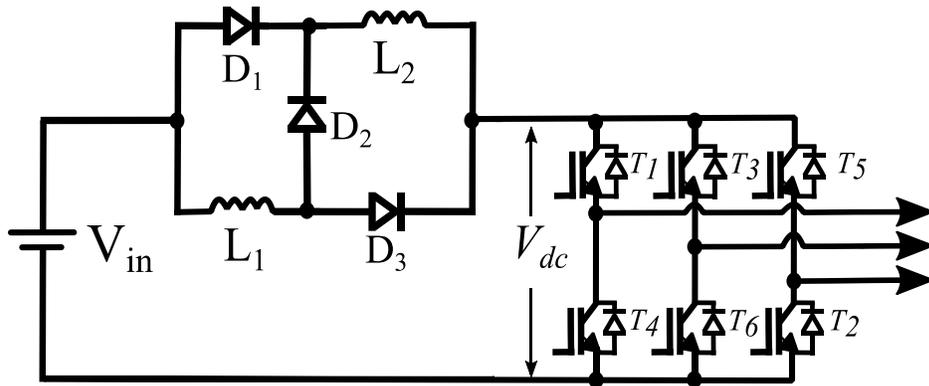


Figure 2.15: L-Z-Source Inverter [22].

In applications with a high boost factor, increasing the number of inductors increases the cost and volume of the system.

The impedance network of this converter has generalizability. Adding an inductor and three diodes in each step increases the boosting factor of the converter. The general topology of the converter for the n^{th} step of generalization is shown in Figure 2.16.

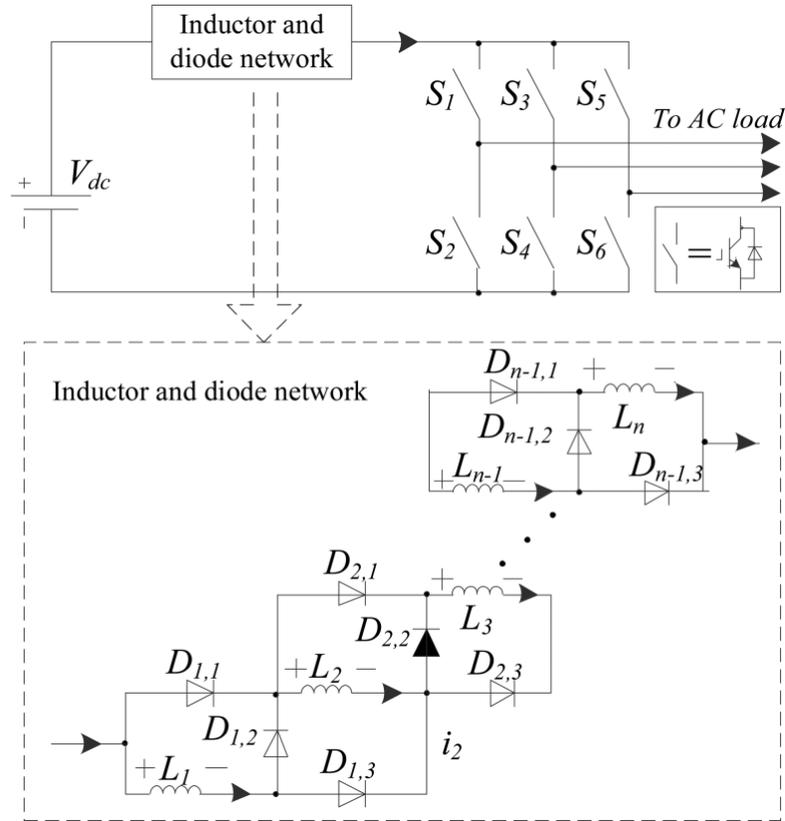


Figure 2.16: The n^{th} step of generalization in the L-Z-Source Inverter impedance network [22].

The general relations of the converter are as follows:

$$B = \frac{1 + (N - 1)D}{1 - D} \quad (2.42)$$

$$\hat{v}_{ac} = M \cdot \frac{\hat{v}_i}{2} = M = \frac{1 + (N - 1)D}{1 - D} \cdot \frac{V_{dc}}{2} \quad (2.43)$$

In the above relations, N indicates the number of impedance network inductors.

2.3.10 Switched-Coupled-Inductor Quasi Z-Source Inverter (SCL-qZSI)

Figure 2.17 shows that adding a capacitor and two diodes to the converter topology makes it a Quasi Z-Source Inverter converter with high boosting capability. Compared to other converters with the same input and output, this converter with a larger modulation index can generate more gain. This process reduces the voltage

stress of the components and reduces the ripple current of the input inductor. Other features include input current connection, common ground between dc source and inverter bridge, and reduced current at the moment of start [24].

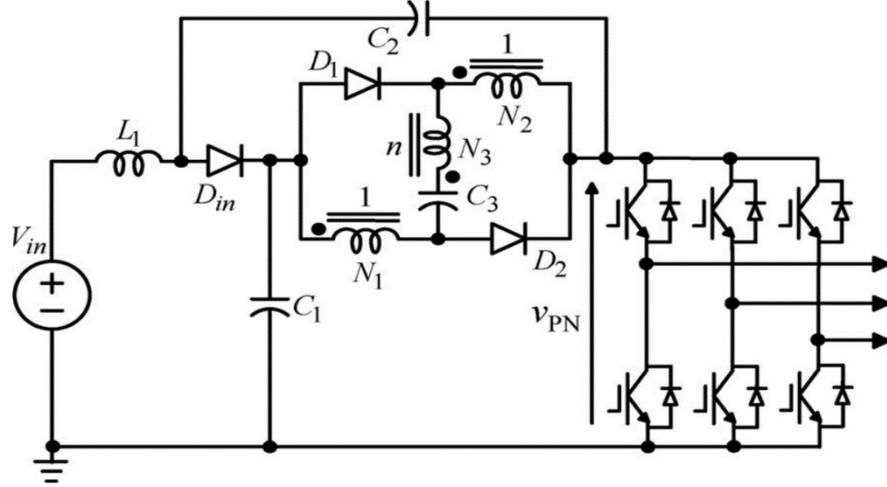


Figure 2.17: Switched-Coupled-Inductor Quasi Z-Source Inverter [24].

The voltage of the network capacitors is calculated based on the following equations:

$$V_{C1} = \frac{1 - D}{n + 1 + D} V_{PN} \quad (2.44)$$

$$V_{C2} = \frac{n + 1 - D}{n + 2} V_{PN} \quad (2.45)$$

$$V_{C3} = \frac{(n + 1)(1 - D)}{n + 2} V_{PN} \quad (2.46)$$

The boost factor of this converter is calculated based on the following equation:

$$B = \frac{V_{PN}}{V_{in}} = \frac{n + 2}{1 - (3 + n)D} \quad (2.47)$$

If n is equal to one, we have:

$$B = \frac{3}{1 - 4D} \quad (2.48)$$

In the relation (2.44) to (2.47), the parameter n is defined as the following relation.

$$n = \frac{N_3}{N_1} = \frac{N_3}{N_2} \quad (2.49)$$

Table 2.2 Summary of Z-network-based ZSI topologies				
Topology	Boost factor	Number of Inductors(L)/Capacitors(C)	Number of Diode	Features
ZSI	$\frac{1}{1-2D}$	2/2	1	<ul style="list-style-type: none"> • lower voltage gain • Start-up inrush current • Discontinuous input current • Lower number of passive components • Higher source voltage stress
qZSI	$\frac{1}{1-2D}$	2/2	1	<ul style="list-style-type: none"> • Continuous input current • Lower source current ripple • No change in the voltage gain
I-ZSI	$\frac{1}{1-2D}$	2/2	1	<ul style="list-style-type: none"> • Continuous input current • Lower source current ripple • Low inrush current
SL-ZSI	$\frac{1+D}{1-3D}$	4/2	7	<ul style="list-style-type: none"> • High boost factor • Discontinuous input current • Higher capacitor voltage stress and start-up inrush current
SL-qZSI	$\frac{1+D}{1-2D-D^2}$	3/2	4	<ul style="list-style-type: none"> • Continuous input current • Reduces the voltage stress on C_2 • Common ground facility • Low boost factor
T-ZSI	$\frac{1}{1-(1+n)D}$	2/1	1	<ul style="list-style-type: none"> • Increased voltage gain • Lower number of passive components • Lower inductor size • Issue with the leakage inductance.
IT-ZSI	$\frac{1}{1-(2+n)D}$	3/2	1	<ul style="list-style-type: none"> • High boosting factor • Continuous input current • Reduce current resonance at the start
Sigma-ZSI	$\frac{1}{1-(2+(\frac{1}{n_{r1}-1})+(\frac{1}{n_{r2}-1}))D_0}$	4/2	1	<ul style="list-style-type: none"> • Increased voltage gain • High transformer volume • Continuous input current
L-ZSI	$\frac{1+(N-1)D}{1-D}$	2/0	3	<ul style="list-style-type: none"> • Increased voltage gain • Elimination of inrush current • Higher voltage gain cannot be achieved without increased component count • Very high ripple content in the inductor currents
SCL-ZSI	$\frac{n+2}{(1-(3+n)D)}$	4/3	3	<ul style="list-style-type: none"> • Increased voltage gain • Lower number of passive components • Lower inductor size

According to the simple boost control method and Equation 3.9, the relation of boost factor, output phase voltage and voltage gain is calculated based on the modulation index:

$$B = \frac{3}{4M - 3} \quad (2.50)$$

$$\hat{v}_{ph} = \frac{MV_{PN}}{2} = \frac{MBV_{in}}{2} \quad (2.51)$$

$$G = \frac{\hat{v}_{ph}}{(V_{in}/2)} = \frac{3M}{4M - 3} \quad (2.52)$$

Table 2.2 shows the summary of ZSI topological improvements. This table includes the number of components, boost factor, and features.

2.4 Conclusion

There is a vast area of research to study the properties of impedance source converters with switched networks. As a result, over the past several decades, it has gained considerable attention from researchers. The purpose of this chapter was to describe the different topologies of Z-Source Inverters and to evaluate their advantages and disadvantages. A lot of efforts and contributions have been made by the experts since the first introduction of the switched inductor Z-source model. Several switched ZSI topologies, structures, configurations, and models have been outlined in this survey, including the basic switched inductor ZSI, two-switched inductor/capacitor ZSIs, and active switch boost ZSIs. Regardless of their impedance configurations, switched ZSIs can be configured to operate as single- or three-phase inverters.

Chapter 3

Controls of converters

3.1. Control of Multi-level inverters

Power electronics converters operate primarily in "switch mode". This means that the switch inside the converter is always in one of two conditions: off (no current) or on (saturated with a slight voltage drop across the switch). Except for the inevitable transition from conductive to non-conductive, operation in the linear region is accompanied by an undesired efficacy loss and an unacceptable increase in switching power loss. The switch substitutes amongst these dual conditions (that is, on and off) regulate the current flowing through the converter. This abundantly occurs fast for the capacitors and inductors on the output and input nodes of the converter to average or filters the switching signal. The converted constituent is diminished to retain the desired DC or low-frequency AC component. This process is called Pulse Width Modulation (PWM) this is because the required mean is controlled by modulating the pulse width.

The switching frequency f_c should be a multiple of the frequency of the preferred basic AC component f_1 for the highest switching component weakening found at the input or output terminals. This contradicts the upper limit for large converters imposed on the switching frequency by switching loss. The ratio of switching frequency to the fundamental frequency f_c/f_1 ($= N$, the number of pulses) with the GTO converter can be reduced to 1. This is identified as square wave switching. Another application that may have a lower number of pulses is a converter, enhanced description as an amplifier [1], whose upper limit basic output frequency can be comparatively elevated. These high-performance switching amplifiers are used in dynamic power filtering, audio amplifiers, servos, and test signal generation [2]. Due to the low pulse counts which impose the highest demands on active modulation to decrease the alteration as much as possible. In such situations, multi-level converters can significantly decrease falsification by astounding the switching cycles of the multi-switch and growing the ostensible number of pulses across the converter. Figure 3.1 shows classification of multilevel inverter modulation techniques. The

advantages of PWM are:

- PWM simplifies output voltage control rather than other methods and does not require any additional parts.
- The lower order harmonics are reduced or completely removed,
- Because lower order harmonics are removed and higher order harmonics are simple to filter, the amount of filtering necessary is reduced.
- Power consumption is very low,
- PWM reduces the susceptibility of the control circuit to interference since the entire circuit can be digitized.

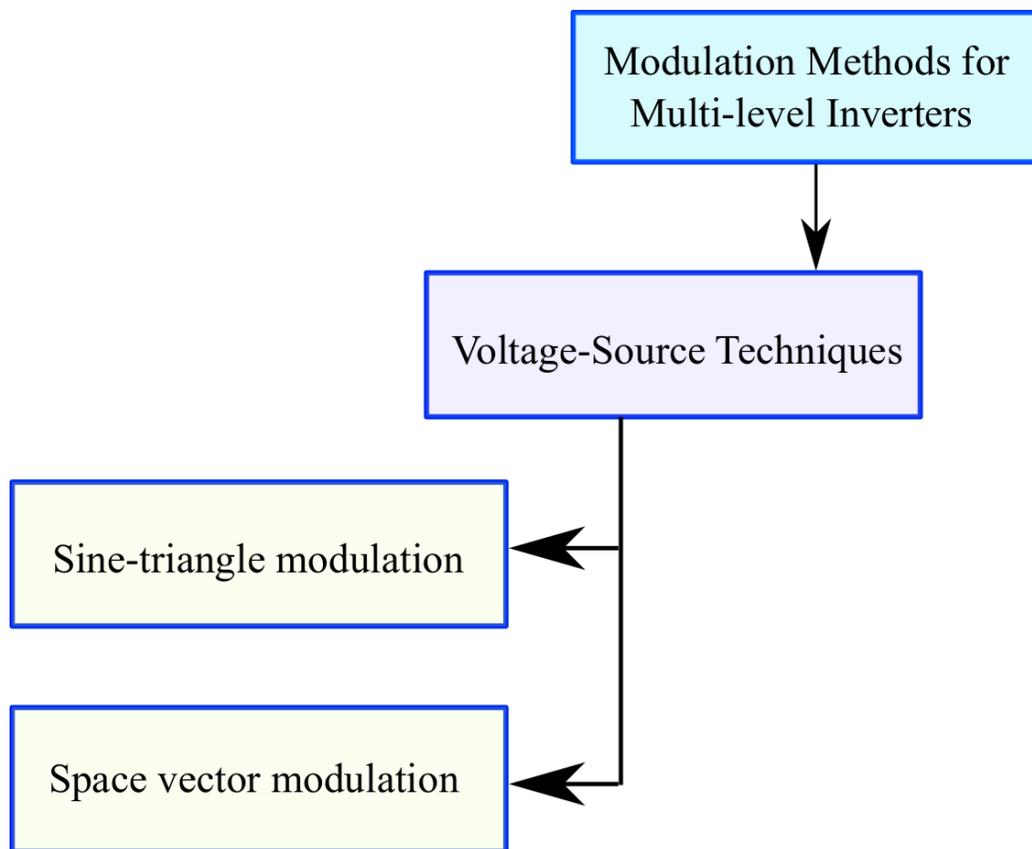


Figure 3.1 Classification of multilevel inverter modulation techniques

3.2. PWM methods

The basic technique of pulse width modulation (PWM) can be categorized into the conventional voltage source and current control techniques. The voltage source scheme is suitable for applying digital signal processors (DSP) or programmable logic devices (PLD). Nevertheless, power controls usually rely event schedule, so it is an analog implementation that can only operate consistently up to a particular level of power. The harmonic performance is not as good as that of voltage-source systems in discrete current-regulated techniques. A basic PWM technique is demonstrated in figure 3.2. The output voltage of inverter can be found according below comparisons:

- When the $V_{control} > V_{tri}$ the output is $V_{dc}/2$
- When the $V_{control} < V_{tri}$ the output is $-V_{dc}/2$

The frequency of $V_{control}$ and V_{tri} are the same. Fundamental frequency and amplitude are adjusted by frequency and maximum value of $V_{control}$; respectively.

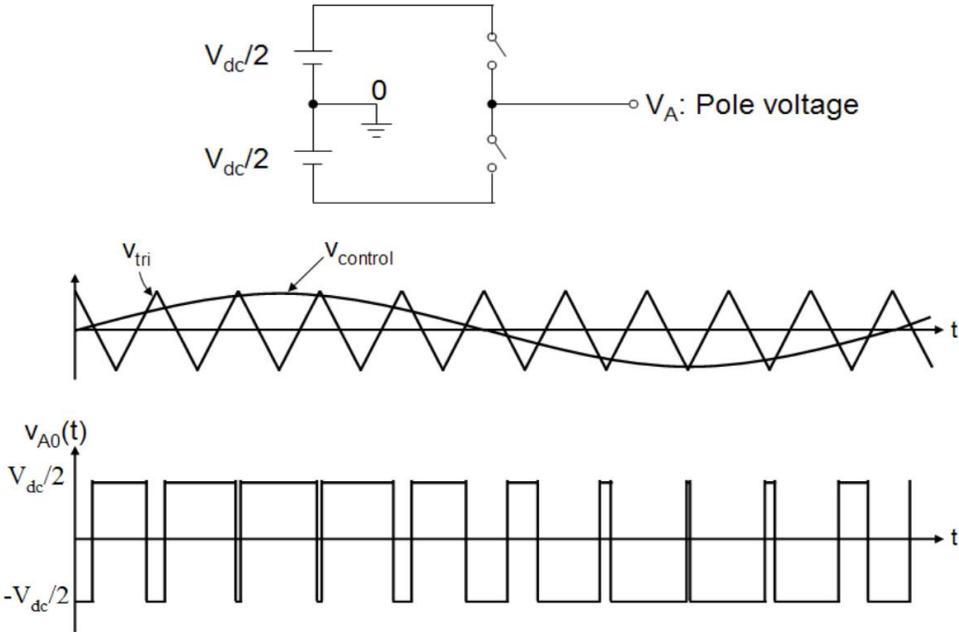


Figure 3.2. Basic method PWM

The index of modulation is defined as:

$$m = \frac{v_{control}}{v_{tri}} = \frac{\text{peak of } (V_{AO})_1}{V_{dc/2}} \quad (3.1)$$

In this formula, $(V_{AO})_1$ is basic frequency of V_{AO} .

3.2.1 Voltage-Source techniques

There are two main paths to voltage-source modulation. Sine-triangular modulation within the cycle of domain and spatial vector modulation in the q-d stationary reference system. Modulation of sine triangles and space vectors is precisely correspondent in each respect. Modifying approximate parameters of the sine-triangle system is similar to regulating other parameters of the spatial vector system.

The interphase voltage of the inverter can be altered directly via the switching condition. For certain inverters, the switching condition is broken down into transistor signals. Nonetheless, it is more required to adjust the line voltage of the load as a control goal. The standard terms comprise DC offset and all third harmonics are in a three-phase system. The commanded line-to-ground voltages will be demarcated to constrict the potentials herein as:

$$\begin{bmatrix} V_{ag}^* \\ V_{bg}^* \\ V_{cg}^* \end{bmatrix} = \frac{mV_{dc}}{2} \begin{bmatrix} \cos(\theta c) \\ \cos(\theta c - \frac{2\pi}{3}) \\ \cos(\theta c + \frac{2\pi}{3}) \end{bmatrix} + \frac{V_{dc}}{2} \left[1 - \frac{m}{6} \cos(3\theta c) \right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (3.2)$$

where m is the modulation index which has a range of $0 \leq m \leq 2/\sqrt{3}$ and θc is the converter electrical angle.

In formula 3.2, the first set of terms on the right defines a sine-wave set of command voltages with amplitudes and frequencies that can be controlled by m and

θc respectively. The second term group on the right is the regular-mode term. In this case, a DC offset is applied and the instructed interphase voltage is within the acceptable range of 0 to the DC voltage. Another common mode term is the third harmonic component that is added to use the DC supply voltage completely. The common-mode term is a minimal set and can direct other types of interphase voltage, comprising discontinuous waveforms to boost switching frequencies or harmonics.

In order to describe the modulation methods, some fundamental definitions will be presented. Initially, the duty cycle is produced by changing and scaling the commanded voltage, and considering multiple voltage levels. The formula of duty cycles:

$$\begin{bmatrix} d_{am} \\ d_{bm} \\ d_{cm} \end{bmatrix} = \left(\frac{n-1}{2}\right) \begin{bmatrix} m\cos(\theta c) \\ m\cos(\theta c - \frac{2\pi}{3}) \\ m\cos(\theta c + \frac{2\pi}{3}) \end{bmatrix} + \frac{n-1}{2} \left[1 - \frac{m}{6} \cos(3\theta c)\right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (3.3)$$

then, a commanded voltage vector is specifying by

$$V^{s*}_{qds} = V^{s*}_{qs} - jV^{s*}_{ds} \quad (3.4)$$

where in fact the voltages in the q- and d-axis are going to be associated with the a-b-c variables of equation 3.2.

$$V^{s*}_{qs} = \frac{2}{3}V^*_{ag} - \frac{1}{3}V^*_{bg} - \frac{1}{3}V^*_{cg} \quad (3.5)$$

$$V^{s*}_{ds} = \frac{1}{\sqrt{3}}(V^*_{cg} - V^*_{bg}) \quad (3.6)$$

Note that the required line-to-line voltage can also describe the Q-axis and J-axis command voltages, as the zero sequences are neglected.

3.2.1.1 Sine-triangle modulation

In the sine-delta technique, for N-level inverters, the a -phase duty cycle is compared to the triangular waveform (usually $n-1$) [3]. Following are the rules for switching:

$$S_{ai} = \begin{cases} 1, & d_{am} > tri \\ 0, & \text{elsewise} \end{cases} \quad (3.7)$$

$$S_a = \sum_{i=1}^{n-1} S_{ai} \quad (3.8)$$

In general, the sine triangle modulation is discussed here for a three -phase inverter.

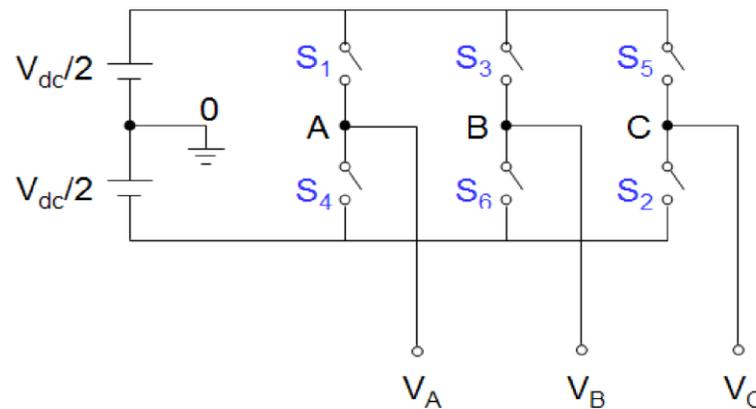


Figure 3.3. 3-phase Sine wave PWM inverter[3].

One way to describe voltage source modulation is to represent the connection of a modulated signal (duty cycle) and a triangular waveform.

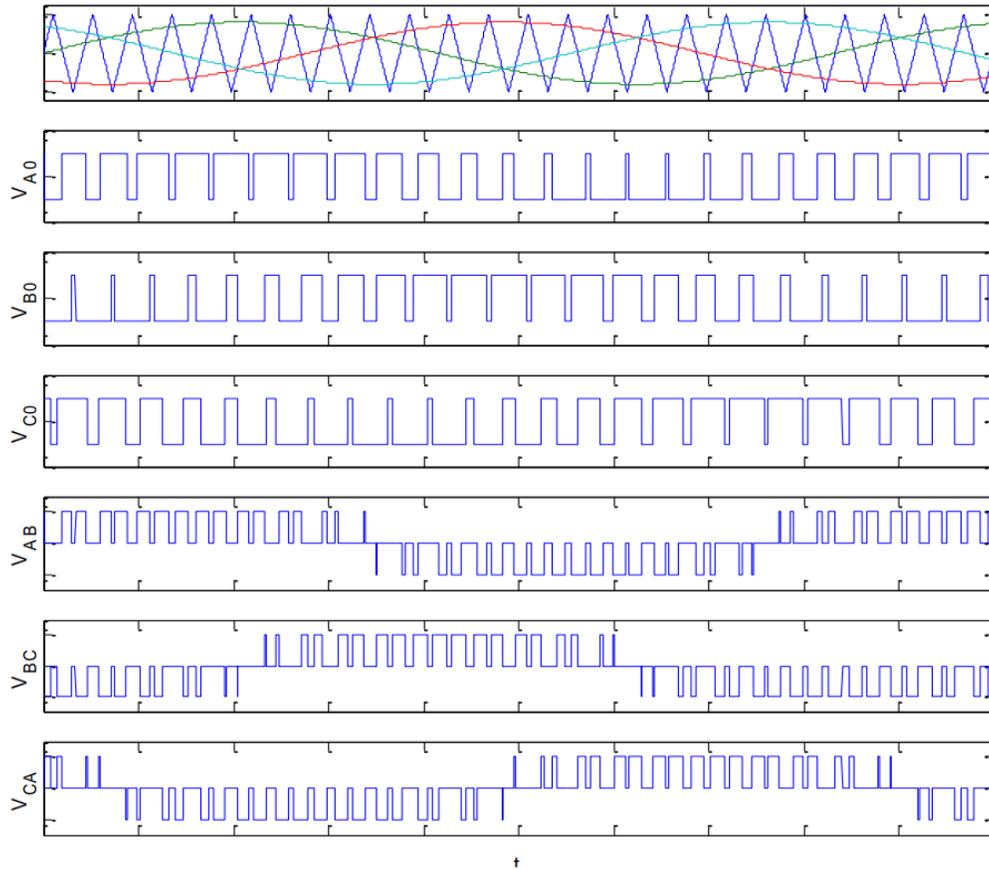


Figure 3.4. Waveforms of three-phase SPWM inverter [3].

Consider, frequency of $v_{tri} = f_s = \text{PWM frequency}$ and frequency of $v_{control} = f_1 = \text{fundamental frequency}$. In Figure 3.4 we have $V_{AB} = V_{A0} - V_{B0}$, $V_{BC} = V_{B0} - V_{C0}$ and $V_{CA} = V_{C0} - V_{A0}$.

Amplitude modulation ratio (m_a) and Frequency modulation ratio (m_f) are given by:

$$m_a = \frac{\text{peak of } (V_{A0})_1}{V_{dc}/2}, \text{ and } m_f = \frac{f_s}{f_1} \quad (3.9)$$

where $(V_{A0})_1$, f_s , and f_1 are fundamental frequency component of V_{A0} , $f_s = \text{PWM frequency}$ and $f_1 = \text{fundamental frequency}$; respectively.

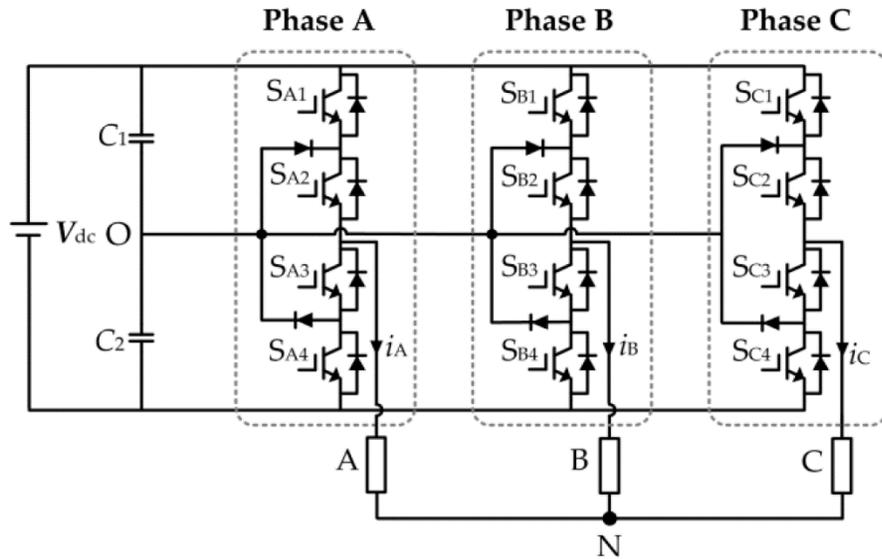


Figure 3.5. Three phase clamped inverter.

In equation (3.9) m_f must be an odd integer. If m is not an integer, there may be fractional harmonics in the output voltage. If m is not odd, there may be a DC component and there are even harmonics in the output voltage. For a three-phase PWM inverter m_f must be a multiplied by three.

Carrier-based modulation systems for multi-level inverters can be broadly divided into 2 groups: Phase shift and level shift modulations. Both modulation systems can be pragmatic to the cascaded H-bridge (CHB) inverters. The phase shift modulation THD is higher than that of level shift modulation. Consequently, we considered level shift modulation. All m -level CHB inverters that use the level shift multi-carrier modulation scheme entail $(m-1)$ triangular carriers with similar frequency and amplitude. $(m-1)$ triangular girders are arranged vertically so that the bands that occupy them are continuous.

For level-shifted multicarrier modulation, there is 3 substitute PWM approaches with dissimilar phase interactions:

- (a) In-phase disposition (IPD), where all carrier waveforms are in phase.
- (b) Phase opposition disposition (POD), all carrier waveforms above 0 reference

are in phase with carrier beneath zero and are 180° degrees out of phase.

(c) In alternate phase disposition (APOD), each carrier is 180° degrees out of phase with the adjacent carrier.

3.2.1.2 Space vector modulation

Spatial vector modulation (SVM) is worked on vector selection in static q-d reference frames [7]. The order voltage vector is described by equation 3.6. The commanded vector is generated with the vector available via the converter. The vector V_{qds}^* of interest is shown at a particular time, but if a 3-phase voltage set across the load is required, it follows a circular path. There are some steps to implement:

- (a) Fulfilment of Space Vector PWM ,
- (b) Transformation: abc to dq ,
- (c) Three phase converter (load voltages)

In the following, the steps are detailed:

The initial step in the SVM system is to determine the three closest vectors:

(a) Fulfilment of Space Vector PWM

Step 1 : Evaluate V_d , V_q V_{ref} , and angle (α)

Step 2 : Evaluate time of T_1 , T_2 , and T_0

Step 3 : Evaluate the switching duration for each IGBT (S_{A1} - S_{A6})

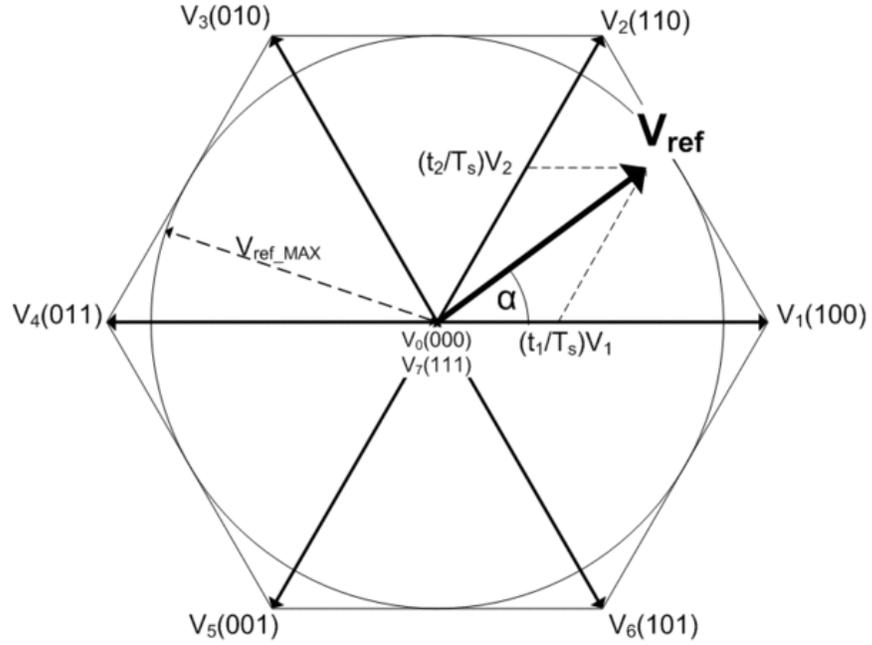


Figure 3.6: Voltage Space Vector and vectors in (d, q).

(b) Transformation: abc to dq

$$V_d = V_{an} - V_{bn} \cdot \cos\left(\frac{\pi}{3}\right) - V_{cn} \cdot \cos\left(\frac{\pi}{3}\right) = V_{an} - \frac{1}{2}V_{bn} - \frac{1}{2}V_{cn} \quad (3.10)$$

$$V_q = 0 + V_{bn} \cdot \cos\left(\frac{\pi}{6}\right) - V_{cn} \cdot \cos\left(\frac{\pi}{6}\right) = V_{bn} + \frac{\sqrt{3}}{2}V_{bn} - \frac{\sqrt{3}}{2}V_{cn} \quad (3.11)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (3.12)$$

$$|\vec{V}_{ref}| = \sqrt{V_d^2 + V_q^2} \quad (3.13)$$

$$a = \tan^{-1}\left(\frac{V_q}{V_d}\right) = \omega_s t = 2\pi f_s t \quad (3.14)$$

where, f_s is fundamental frequency. The switching time interval in sector 1 is calculated:

$$\int_0^{T_z} \bar{V}_{ref} = \int_0^{T_1} \bar{V}_1 dt + \int_{T_1}^{T_1+T_2} \bar{V}_2 dt + \int_{T_1+T_2}^{T_z} \bar{V}_0 \quad (3.15)$$

$$T_z \cdot \bar{V}_{ref} = (T_1 \cdot \bar{V}_1 + T_2 \cdot \bar{V}_2) \quad (3.16)$$

$$T_z \cdot |\bar{V}_{ref}| \cdot \begin{bmatrix} \cos(a) \\ \sin(a) \end{bmatrix} = T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix} \quad (3.17)$$

$$\text{where } 0 \leq \alpha \leq \frac{\pi}{3}$$

$$T_1 = T_z \cdot a \cdot \frac{\sin(\frac{\pi}{3} - a)}{\sin(\pi/3)} \quad (3.18)$$

$$T_2 = T_z \cdot a \cdot \frac{\sin(a)}{\sin(\pi/3)} \quad (3.19)$$

$$T_0 = T_z - (T_1 + T_2), \left(\text{where, } T_z = \frac{1}{f_s} \quad \text{and} \quad a = \frac{|\bar{V}_{ref}|}{\frac{2}{3} V_{dc}} \right) \quad (3.20)$$

Switching time duration at any Sector is shown below

$$\begin{aligned} T_1 &= \frac{\sqrt{3} T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(\sin \left(\frac{\pi}{3} - a + \frac{n-1}{3} \pi \right) \right) \\ &= \frac{\sqrt{3} T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(\sin \frac{n}{3} \pi - a \right) \\ &= \frac{\sqrt{3} T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(\sin \frac{n}{3} \pi \cos a - \cos \frac{n}{3} \pi \sin a \right) \end{aligned} \quad (3.21)$$

$$\begin{aligned} T_2 &= \frac{\sqrt{3} T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(\sin \left(a - \frac{n-1}{3} \pi \right) \right) \\ &= \frac{\sqrt{3} T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(-\cos a \cdot \sin \frac{n-1}{3} \pi + \sin a \cdot \cos \frac{n-1}{3} \pi \right) \end{aligned} \quad (3.22)$$

$$T_0 = T_z - T_1 - T_2 \quad (3.23)$$

In these equations, $n = 1$ through 6 (which is sector 1 between sector 6), $0 \leq \alpha \leq \frac{\pi}{3}$. A power converter with three phase output voltage is shown:

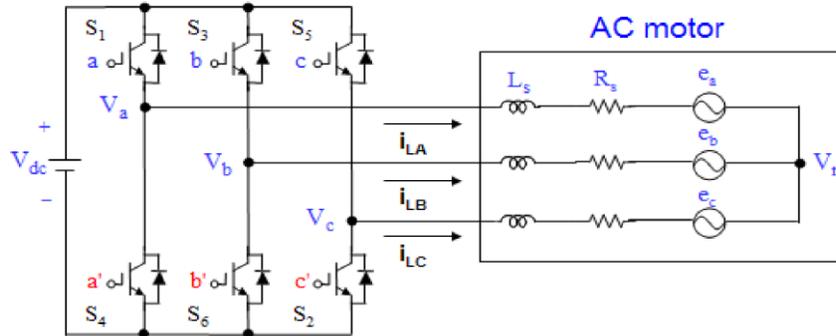


Figure 3.7 Power converter with three phase output voltage

Table 3.1 Switching pattern at each sector

Sector	Top switches (S_1 , S_3 , S_5)	Bottom switches (S_4 , S_6 , S_2)
1	$S_1 = T_1 + T_2 + T_{0/2}$ $S_3 = T_2 + T_{0/2}$ $S_5 = T_{0/2}$	$S_4 = T_{0/2}$ $S_6 = T_1 + T_{0/2}$ $S_{20} = T_1 + T_2 + T_{0/2}$
2	$S_1 = T_{10} + T_{0/2}$ $S_3 = T_1 + T_2 + T_{0/2}$ $S_5 = T_{0/2}$	$S_4 = T_2 + T_{0/2}$ $S_6 = T_{0/2}$ $S_2 = T_1 + T_2 + T_{0/2}$
3	$S_1 = T_{0/2}$ $S_3 = T_1 + T_2 + T_{0/2}$ $S_5 = T_2 + T_{0/2}$	$S_4 = T_1 + T_2 + T_{0/2}$ $S_6 = T_{0/2}$ $S_2 = T_1 + T_{0/2}$
4	$S_1 = T_{0/2}$ $S_3 = T_1 + T_{0/2}$ $S_5 = T_1 + T_2 + T_{0/2}$	$S_4 = T_1 + T_2 + T_{0/2}$ $S_6 = T_2 + T_{0/2}$ $S_2 = T_{0/2}$
5	$S_1 = T_2 + T_{0/2}$ $S_3 = T_{0/2}$ $S_5 = T_1 + T_2 + T_{0/2}$	$S_4 = T_1 + T_{0/2}$ $S_6 = T_1 + T_2 + T_{0/2}$ $S_2 = T_{0/2}$
6	$S_1 = T_1 + T_2 + T_{0/2}$ $S_3 = T_{0/2}$ $S_5 = T_1 + T_{0/2}$	$S_4 = T_{0/2}$ $S_6 = T_1 + T_2 + T_{0/2}$ $S_2 = T_2 + T_{0/2}$

The top transistors are S_1 , S_3 , S_5 , bottom transistors: S_4 , S_6 , S_2 , and switching

variable vectors are a , b , and c . The duration of switching for every transistor ($S_j - S_6$) is indicated in Table 4.1.

(c) Three phase converter (load voltages)

The six switches, S_1 to S_6 are which generate the output load voltage. While one of top switch is on state (i.e., $a=1$), the corresponding lower switch is turned off (i.e., $a'=0$). The voltage vector (L-L) is $[V_{ab} \ V_{bc} \ V_{ca}]^t$. In this matrix, voltage vectors consists of $[a, b, c]$:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{3.24}$$

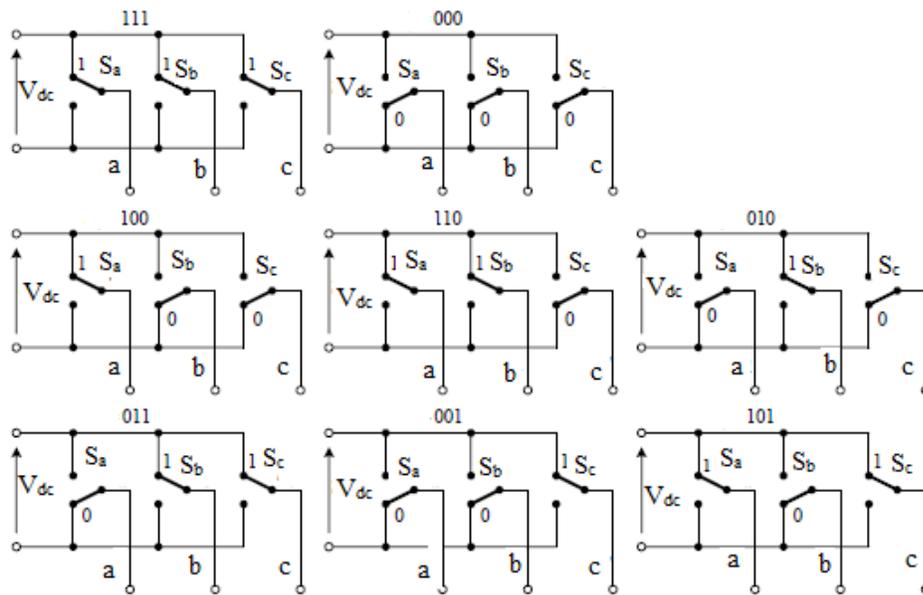


Figure 3.8. Switching states of power converter (three phase).

The phase voltage (L-n) vector $[V_{an} \ V_{bn} \ V_{cn}]^t$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3.25)$$

Figure 3.8 are illustrate output voltage vectors for each state. The combinations states, voltages (L-L, and L-n) are presented in table 3.2.

Table 3.2. Output Voltage (L-n, L-L) in SVM

Vectors	State Vectors			L-n voltage			L-L voltage		
	a	b	c	V _{an}	V _{bn}	V _{cn}	V _{ab}	V _{bc}	V _{ca}
V ₀	0	0	0	0	0	0	0	0	0
V ₁	1	0	0	2/3	-1/3	-1/3	1	0	-1
V ₂	1	1	0	1/3	1/3	-2/3	0	1	-1
V ₃	0	1	0	-1/3	2/3	-1/3	-1	1	0
V ₄	0	1	1	-2/3	1/3	1/3	-1	0	1
V ₅	0	0	1	-1/3	-1/3	2/3	0	-1	1
V ₆	1	0	1	1/3	-2/3	1/3	1	-1	0
V ₇	1	1	1	0	0	0	0	0	0

3.3 Control of Z-Source Inverter

Impedance-source networks can be characterized as two-port networks with two linear passive components, typically L and C (a dissipative component R is usually omitted). The impedance network also can be modified by adding different nonlinear elements, e.g., diodes, switches, and/or a combination of both, to improve the circuit performance. As a result of limitations associated with voltage source inverters (VSI) and current source inverters (CSI), which are used mostly in electric power conversion, the impedance-source network was invented [10]. Unlike conventional inverters, the shoot-through condition can be utilized in the Z-source inverter regulation to increase voltage. The shoot-through interval control has been meticulous as in [11-13]. Figures 3.9 shows the conventional and main topology of Z-source inverter, which is connected to load.

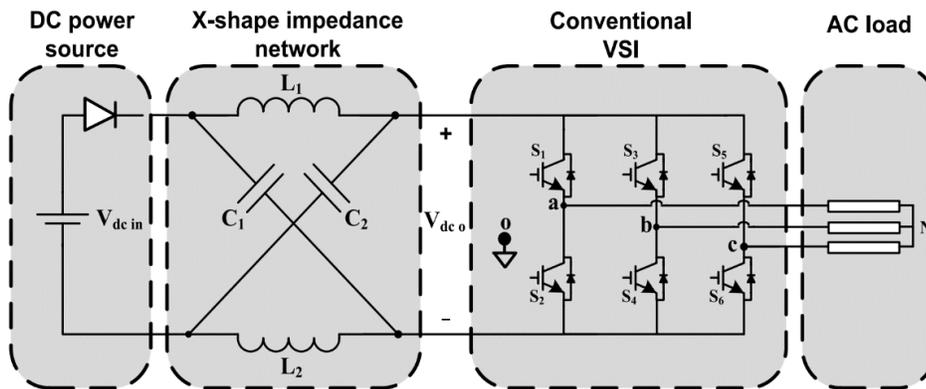


Figure 3.9 Z-Source inverter[11].

3.3.1 Classification of General Modulation Techniques

The amalgamation of traditional switching models together with a choosy shoot-through condition might be achieved by the superlative modulation methods to boost maximization, the harmonic distortion minimization, decrease the switches pressure, and cut the device commutations figure in each switching period. Figure 3.10 portrays an electrical power conversion system based on an impedance-source grid with various switching configurations. Numerous combination plans using an impedance source inverter offer broad electric power conversion topologies from medium current /voltage to high current/voltage. Therefore, using this switching configuration for isolated/non-isolated, bidirectional/unidirectional converters can employ for any sort of converters (AC-AC), (DC-DC), inverter (DC-AC), and rectifier (AC-DC).

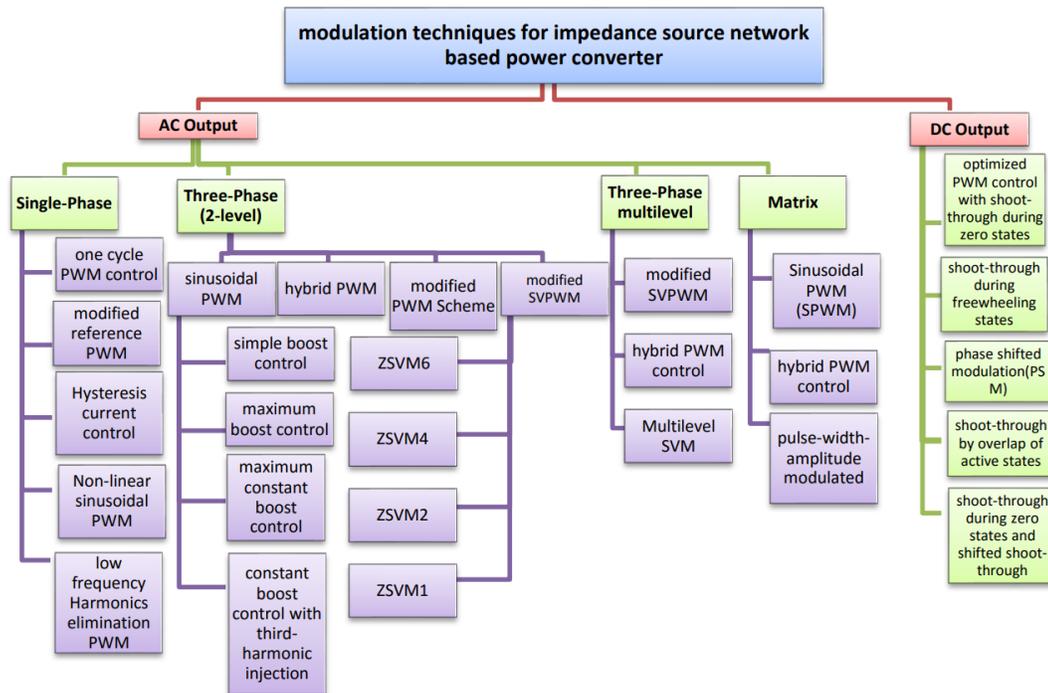


Figure 3.10. Classification of modulation techniques for the impedance-source network [4].

3.3.1.1 Modulation systems for single-phase topologies

Several modulation methods are introduced in the literature to modify and regulate the output voltage of single-phase impedance source inverters partaking two switches for quasi-Z-source and semi Z-source [5-6, 8], four-switches intermediary H-bridge topologies [9, 10], for numerous solicitation. For a single-phase grid-connected photovoltaic system, a two-switch topology offers a modest but worthwhile resolution.

To obtain the required output voltage, two modulation methods, one-cycle control [8] and Nonlinear Sinusoidal Pulse Width Modulation (SPWM), predominate in the literature for adjusting and modifying two Z-source-like switches and a single-phase Z-source [6].

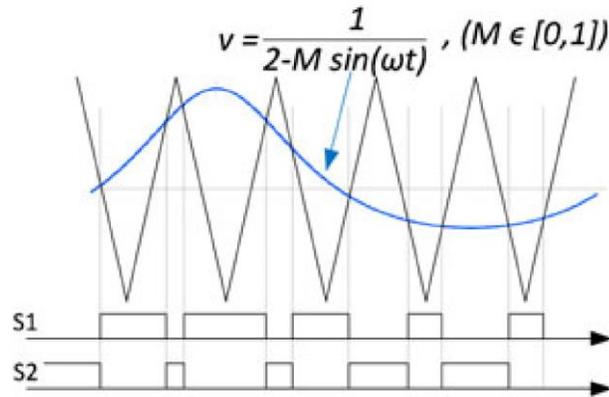


Figure 3.11 Nonlinear sinusoidal pulse width modulation (SPWM) [4].

In quasi-Z-source and semi-Z-source converters, comparing the non-linear sinusoidal references signal $v = [2 - M \sin(\omega t)]^{-1}$ with the carrier signal is required to provide a switch drive signal, as shown in Figure 3.11. A matching modulation technique named a single-phase stabilized Z-source converter with four switches is presented [11]. To adjust the single-phase semi-Z-source topology a one-cycle control technique was used [8]. The two switches work in tandem, where the clock signal (CLK) is used to turn on each of the switches specified in this control method. The incorporated voltage through the switches can turn the switch gate ON and as the voltage reaches to signal $(v_r - v_{ref})$, the integrator will turn OFF the switch as shown in Figure 3.12.

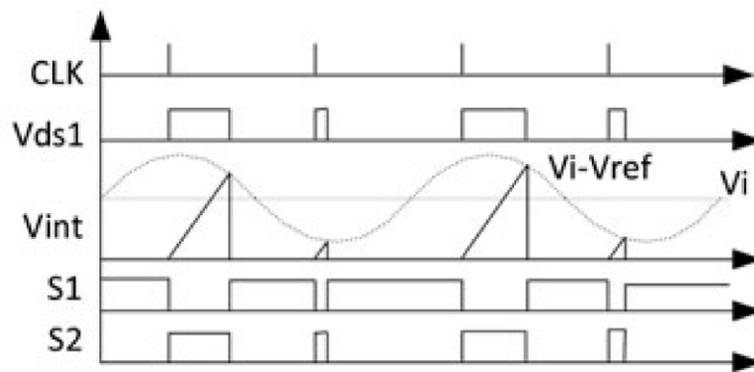


Figure 3.12 Generation of switching signal for 1-ph Z-source inverter using one cycle control method (Max Y-axis is one-Control signals) [4].

This control technique eliminates input disturbances and is impervious to the conceptual framework, resulting in stable, high-efficiency persistent-frequency control. Poh Chiang et al. [9] modified a standard carrier-based PWM for a single-phase H-bridge topology. As shown in Figure 3.13, a shoot-through duty cycle is used as an alternative to the zero condition without changing the average volt-sec voltage.

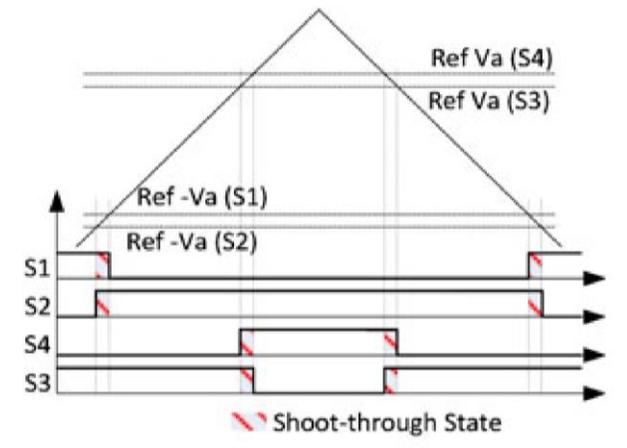


Figure 3.13 Modified space vector modulation SVM [4].

Similarly, to conventional sinusoidal SPWM, the active condition in the respective switching cycle is reserved. As a result, the output waveforms remain sinusoidal. However, they increased to the desired level by precisely regulating the shoot-through period. In both continuous and intermittent modes, the modulation index is drawn out to three-phase/four-phase H-bridge topologies for a voltage-fed impedance network. In addition, [10] have presented the existing hysteresis band design for H-bridge. The performance of both proportionate and disproportionate Z-source networks is verified. Similarly, a low-frequency harmonics elimination PWM approach is introduced in the modulation method used [12-13] for a three-phase inverter, which has the distinct characteristics of decreasing the size, output harmonic distortion, and system cost [14]. Also a modified Z-source with two switches proposed in [15], which lowers circuit cost. Table 4.3 summarizes the modified modulation techniques revised for single-phase impedance grid-based converters.

Table 3.3 An analysis of different modulation techniques for topologies based on a single phase

Modulation methods	Switching Structure	Number of Switches	Maximum Stress on Devices	Modulating sinusoidal signal	Variation of M and D_{st}	Characteristic
Nonlinear SPWM [8]	Semi Z-Source	Two	$\hat{V}_{pn} = 3V_{in}$ $\hat{I}_{pn} = 3I_{in}$	One quasi	$0 \leq M \leq 1$ And $0 \leq D \leq 1$	<ul style="list-style-type: none"> • Remove leakage current • Cost-effective solution • High stress on devices • Restricted to two switch impedance network topologies
One-cycle	Single-phase	Two	$\hat{V}_{pn} = 3V_{in}$ $\hat{I}_{pn} = 3I_{in}$	One	$\frac{1}{3} \leq D \leq 1$	<ul style="list-style-type: none"> • Possible work in Constant frequency control • Higher stress on devices • Restricted to two switch impedance network topologies
Carrier Based PWM [11]	H-bridge	Four	$\hat{V}_{pn} = BV_{in}$ $\hat{I}_{pn} = B\hat{i}_o$	Two	$0 \leq M \leq 1$ And $0 \leq D_{st} \leq 0.5$	<ul style="list-style-type: none"> • Modulation methods possible extend to N-phase inverter.
Hysteresis-Band Current Control [12]	H-bridge	Four	$\hat{V}_{pn} = BV_{in}$ $\hat{I}_{pn} = B\hat{i}_o$	A band of sinusoidal	$0 \leq D_{st} \leq 0.5$	<ul style="list-style-type: none"> • applicable for symmetric or asymmetric network structures • high quality waveform of output current • Simple, robust • Higher device stress due to no uniform switching • Switching frequency is not regular

3.3.1.2 Three-Phase Topology Modulation Techniques (2-level)

This part discussed the dissimilar pulse width modulation techniques to reduce the voltage pressure, easy implementation, and commutation times. Space Vector Pulse Width Modulation (SVPWM) and sinusoidal SPWM are the most common two-level modulation methods, and various modifications such as maximum boost, simple amplification, maximum constant amplification, and constant amplification by third harmonic injection are introduced [12,16]. Multiple SVPWM control methods for voltage increase communication were introduced in [13, 17]. The most important

standard is simple boost control, which is derived from conventional sinusoidal SPWM and involves comparing a three-phase reference signal with a triangular carrier signal for sine output voltage and two straight lines (V_p and V_n) to generate shoot-through for voltage boost, as shown in Figure 4.14. Nonetheless, by decreasing the modulation index, the shoot-through time increases instantly.

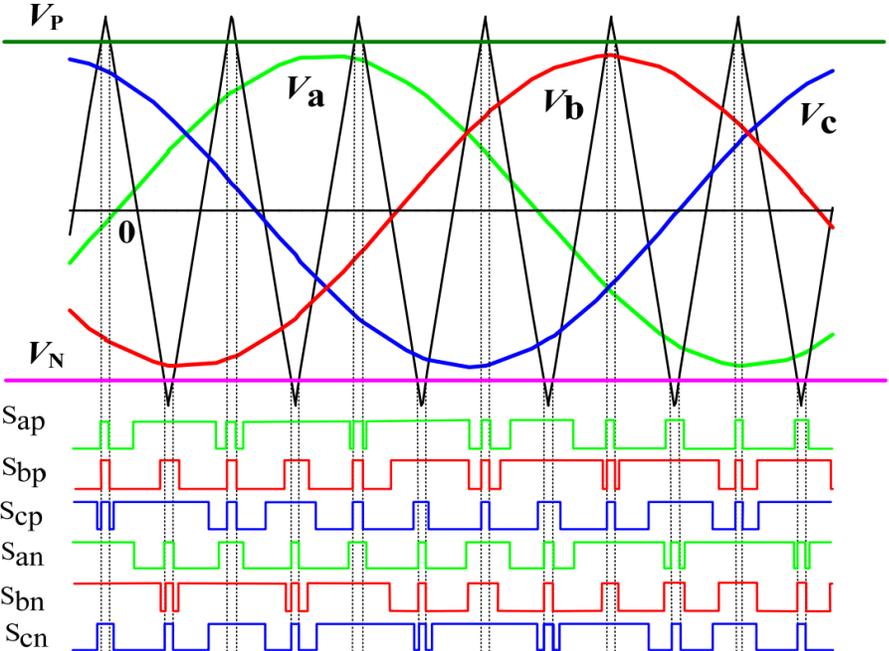


Figure 3.14 Simple boost control method

The primary disadvantage of the modulation method is the shoot-through period, which is limited to $D_{st\ max} = (1 - M)$ and the boosts factor, which is limited to $B = [2M - 1]^{-1}$. When a higher voltage amplification is required, the modulation technique raises the pressure of the device. Fang Zheng proposed the best method for controlling boost pulse width modulation to overcome this issue [16]. Most boost modulation methods use all zeroes to generate a shoot-through time and maintain six dynamic conditions similar to conventional carrier control, as shown in Figure 3.15. By converting all zeroes into a shoot-through period, the boost factor increases to $B = \pi [3\sqrt{3} - \pi]^{-1}$.

Henceforth, dropping the device's pressure is associated with the simple boost control system. Low-frequency harmonics in the passive part can increase the cost and volume of the circuit as the shooting period changes.

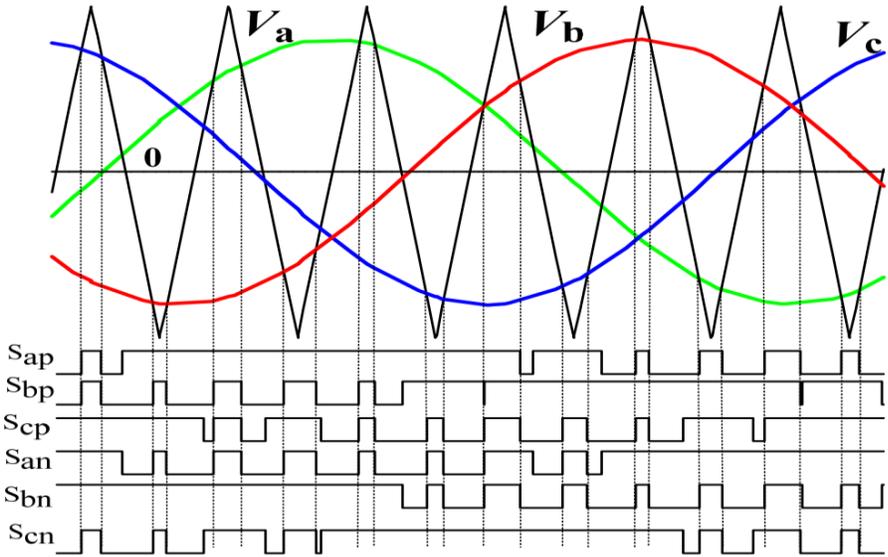


Figure 3.15 Maximum boost control method

The elimination of low-frequency gain in the impedance source network components can have the best amplification feature with a continuous shooting period. A highest constant boost control method is introduced in [12-14]. Figure 3.16 depicts the maximum-constant-boost waveform. Table 3.4 shows a comparison of the highest-constant-boost technique with other sine PWM methods. The comparison of the three-control strategy indicates in Figures 3.17 and the pertinent equation is shown in Table 3.4. The maximum boost control as mentioned in the figure provides the highest voltage gain, whereas the maximum constant boost control offers a bit higher voltage gain than the simple boost control.

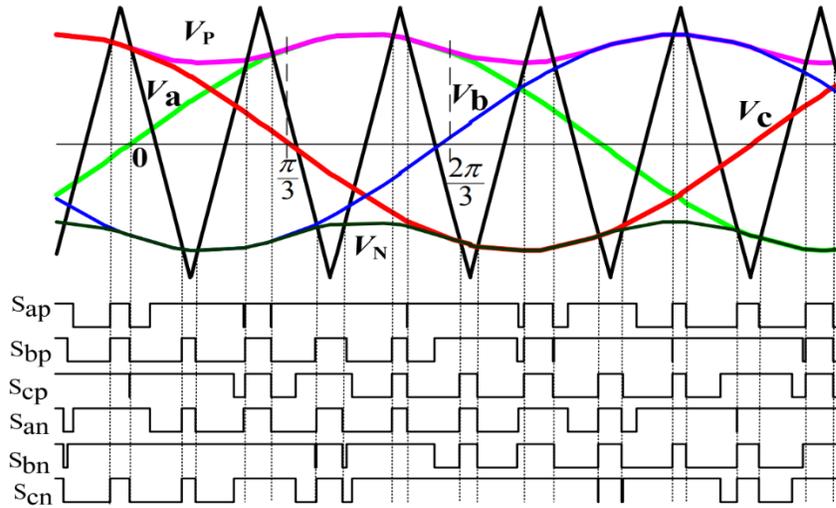


Figure 3.16 Maximum constant boost control method

Table 3.4. SPWM methods for three phase impedance source converter

Control Strategies and its functions	Simple Boost Control	Maximum Constant Boost Control	Maximum Boost Control
Shoot-through Duty Ratio	$\frac{T_0}{T} = 1 - M$	$\frac{T_0}{T} = 1 - \frac{\sqrt{3}M}{2}$	$\frac{\bar{T}_0}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi}$
Boost Factor	$B = \frac{1}{(1 - 2\frac{T_0}{T})}$	$B = \frac{1}{\sqrt{3}M - 1}$	$B = \frac{\pi}{3\sqrt{3}M - \pi}$
Voltage Gain	$G = MB$	$G = \frac{M}{\sqrt{3}M - 1}$	$G = \frac{\pi M}{3\sqrt{3}M - \pi}$
Voltage Stress	$V_s = (2G - 1)V_{dc}$	$V_s = (\sqrt{3}G - 1)V_{dc}$	$V_s = (\frac{3\sqrt{3}G}{\pi} - 1)V_{dc}$
Voltage Stress/ Equivalent DC Voltage	$\frac{V_s}{G V_{dc}} = (2 - \frac{1}{G})$	$\frac{V_s}{G V_{dc}} = (\sqrt{3} - \frac{1}{G})$	$\frac{V_s}{G V_{dc}} = (\frac{3\sqrt{3}}{\pi} - \frac{1}{G})$

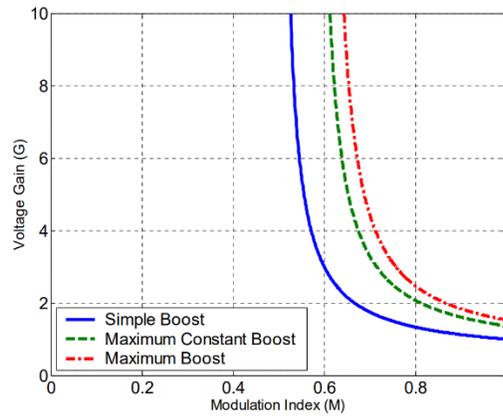


Figure 3.17 Comparison of voltage gain for different modulation techniques

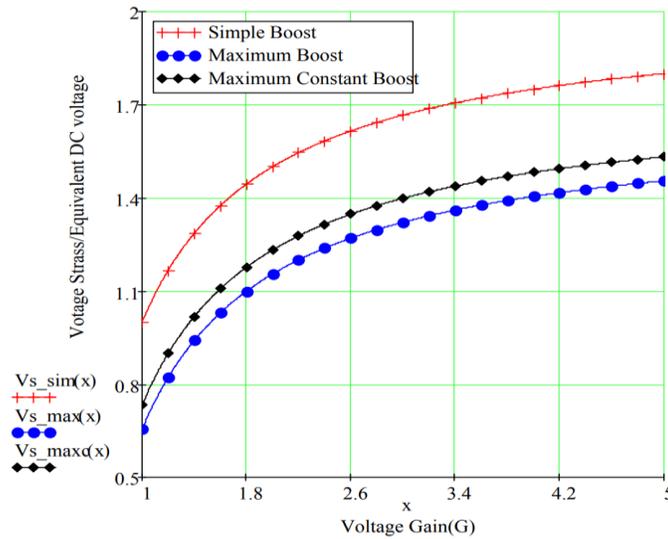


Figure 3.18 Voltage stress comparison for different modulation techniques

Figure 3.18 illustrates the comparison of voltage gain versus voltage stress. It is evident the maximum boost control strategy provides lower voltage stress across the inverter bridge switches. The maximum boost control provides the highest voltage gain and lowest voltage stress across the switch devices.

3.4 Conclusion

Multi-level converters could realize an active upsurge in general switching frequency by canceling the lowermost switching frequency term. This section described dissimilar kinds of carrier-based PWM modulation methods. The PWM technique is beneficial for regulating the output voltage and decreasing the harmonics. Multi-level inverters have numerous modulation techniques. Nonetheless, carrier-based modulation techniques are simple and effective. Multilevel converters are today the preferred solution for high power applications. The most common multilevel converter topologies have been described in this chapter. Complexity both in control and hardware structure, reliability, modularity and efficiency as the most important parameters for high power applications are addressed for the described topologies. Several modulation techniques for multilevel converters have also been briefly reviewed.

In addition, an in-depth analysis of modelling, control, and modulation methods for impedance source networks for power converters has been provided in this section. In order to make choosing control and modulation strategies for suitable structures for specific applications [4]. The modulation techniques have been broadly classified in five with additional subcategories. Besides that, in order to achieve the maximum voltage boost, the least amount of harmonic distortion, the lowest possible semiconductor stress, and the fewest quantity of device commutations for every switching period, it is necessary to compare diverse modulation scheme for specific switching configurations based on mathematical complexity and performance.

Chapter 4

Proposed Multilevel Inverter

4.1 Introduction

Multilevel inverters are applicable in medium voltage and high power applications such as electrical motor drives, energy storage systems, reactive power compensators, and flexible AC transmission systems (FACTS) [1-2]. Nabae first introduced these inverters in 1975, which are comprised of a series combination of multiple neutral point clamped (NPC) three-level full-bridge converters [3-4]. Multilevel inverters can be categorized into three groups: NPC inverters [4], flying capacitor (FC) multilevel inverters [5], and multilevel inverters with cascaded H-full bridges (CHB) [6].

As the most common NPC and FC inverters' failures are related to the unbalanced DC link voltage and the high stress on switches, researchers have focused on CHB converters by providing different structures. These structures can be compared in various aspects, such as the number of levels, the number of DC sources, the number of switches, and the total standing voltage (TSV) [7-8].

Another method to produce multilevel converters is using modules, thus multimodular converters (MMCs) arise. A DC source with two switches can generate a level of this multilevel converter, so it can be considered as a module [9]. If these modules are connected in series, a greater number of levels can be reached. In addition, an auxiliary circuit, such as an H-bridge, can turn these positive levels to negative ones. Thus, a sinusoidal voltage output with no DC component can be obtained [10]. The main drawback is that the switches in the H-bridge circuit must tolerate high voltage stress.

Multilevel converters usually produce a sinusoidal waveform with small output voltage steps. An output voltage step is a DC voltage, which can be added or subtracted to track a sinusoidal waveform. Thus, any multilevel converter's main goals are to minimize the number of components and produce an output voltage with the highest number of levels to reduce the Total Harmonic Distortion (THD) of the output signal.

In order to achieve that, an attractive solution is to use asymmetric DC sources [11-12]. If asymmetric DC sources are used, the voltage stress in each switch is different. The TSV is defined as the maximum voltage applied to each switch during the off state. The lower the TSV, the lower the power losses in the switches. In order to reduce voltage stress, an enhanced H-bridge with different DC sources has been proposed in [13]. However, for improving the voltage and current quality, the converters require more levels; so the number of switches increases. Due to that, in general, cost, conduction and switching losses and complexity of the control system increase, and reliability reduces. Many structures have been introduced to increase the number of voltage levels, in order to improve the system's performance [13-14,16].

Asymmetrical CHB multilevel inverter (CHB-MLI) topologies have been introduced to increase the number of levels by connecting different non-equal voltage DC sources [13–15]. The main drawback is that the switches' stresses are not the same. The voltage stress on switches connected to the highest DC input voltage will be higher than that on switches connected to the lowest DC input voltage. Unbalanced loss sharing among switches will cause varying high temperatures for switches. In addition, unequal voltage stresses mean different voltage ratings will be used for switches, which results in a higher cost. Other modified topologies based on CHB have been proposed to improve the output voltage quality [16-17], but the advantages of the CHB, such as simplicity, simple construction, simple control, and modularity, are lost.

Cascaded structures have also drawn attention because of their advantages compared to the prior topologies, such as simpler control structure and absence of diodes and capacitors for generating more levels in high power applications [14-15]. On the contrary, cascaded structures have some disadvantages, such as the need for multiple DC power sources for each base unit to generate more voltage levels [17,18].

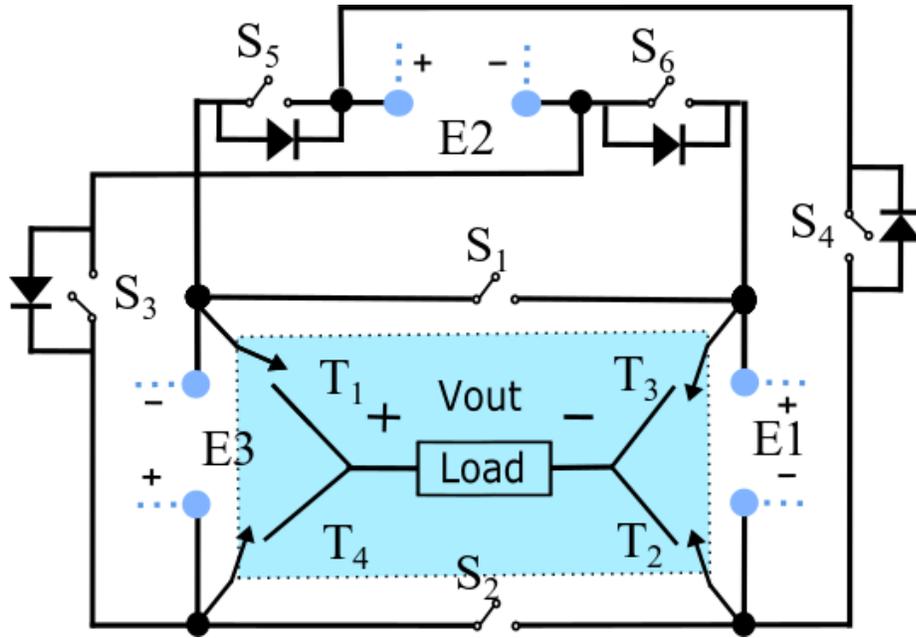
New structures for multilevel inverters such as hybrid and asymmetrical cascaded multilevel structures have recently appeared to decrease the number of input DC voltage sources [19,20]. However, these structures need specific algorithms to determine the amount of DC voltage sources. Furthermore, the presence of too many

switches is not cost-effective. Although the rated voltage of switches may be low in these multilevel inverters, the fact that each switch requires a separate driver and protection circuit increases the cost and complexity of the circuit notably [21].

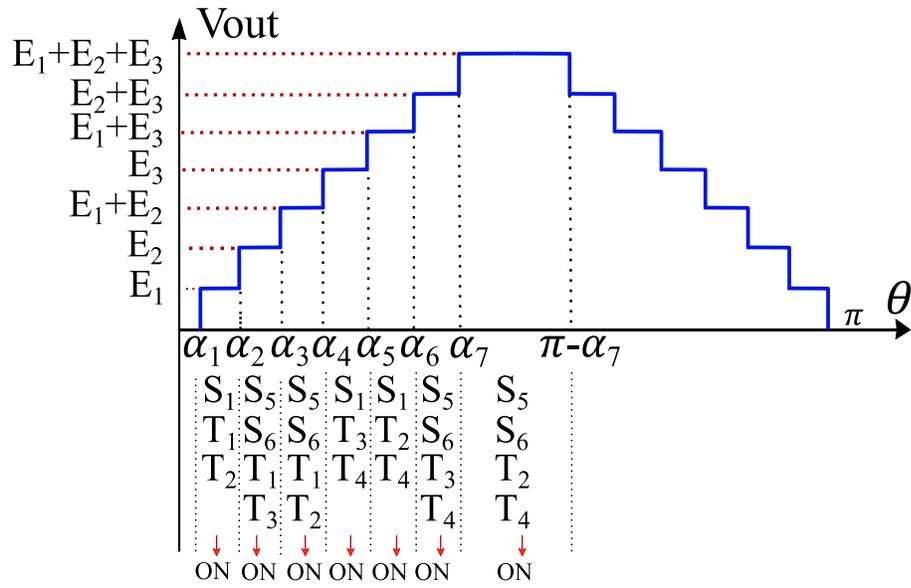
In this chapter, proposes a new structure that aims to reduce construction costs and increase power quality. The proposed structure is analyzed in two parts: single basic unit and cascaded of basic units. The single basic unit needs three DC sources and only ten switches, which can produce a sinusoidal output with 15 levels. This way, the proposed single unit offers a great tradeoff between the number of DC sources, number of switches, and the number of levels, thus producing a very low distortion in the output port. This inverter can be widely used as an interface for renewable energy sources and high-voltage overhead distribution lines [13-14]. In addition, several single basic units can be connected in cascade to reach a higher voltage range and a greater number of levels because the cascaded units can have different DC input voltages and thus can create additional voltage levels control method. Section 4.8 describes how to connect the basic units to create a cascaded structure. Section 4.9 compares the proposed cascaded multilevel inverter with several cascaded multilevel inverters that have been presented in the literature. The simulation and experimental results are investigated and presented in Section 4.10. Finally, the conclusions are shown in Section 4.11.

4.2 Description and analysis of the basic unit

The basic unit of the proposed method is illustrated in Figure 4.1.as for single-phase system and can be extended to produce three-phase system by using three basic units one per phase. The basic structure consists of ten switches: six bidirectional switches (S1, S2, T1, T2, T3, T4), which block the current in the two directions (details of the bidirectional switches are shown in Section 5.2.C), and four unidirectional switches (S3, S4, S5, S6). It has three inputs, E1, E2, and E3, which must be isolated among each other to ensure the proper operation of the converter.



(a)



(b)

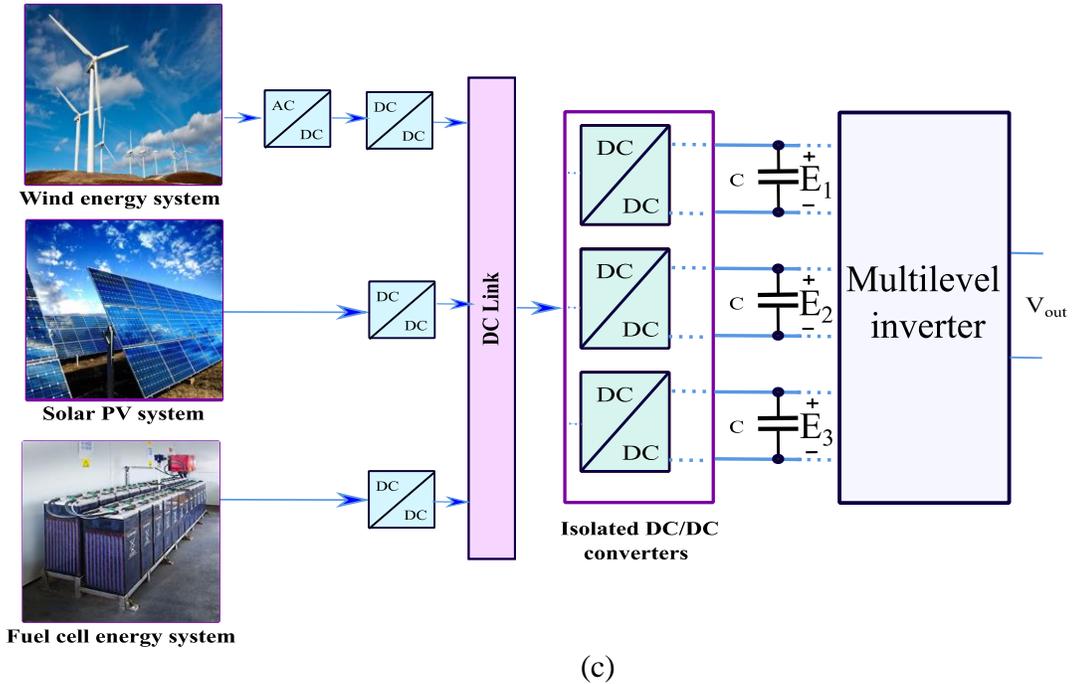


Figure 4.1 Proposed 15-level multilevel converter: (a) basic unit, (b) Switching pattern, (c) Application for renewable sources [18].

The ratio between the DC sources must be:

$$E_2 = 2E_1 \quad \& \quad E_3 = 2E_2 \quad (4.1)$$

in order to minimize of the total harmonic distortion (THD) of the output voltage. The basic structure is shown in Figure 4.1.a, its output voltage has 15 levels: seven positive, seven negative voltage levels and one zero-voltage level. Table 4.1 shows the state of the switches and the corresponding output voltage. In addition, Figure 4.1.b illustrated the switching pattern for each level. Figure 4.1.c shows an application of the multilevel converter using several renewable energy sources as power inputs. This is one of the methods to produce the three independent sources, where a DC link is used and then independent DC/DC converters provides the input DC sources. Another possibility is a direct connection of PV panels using the strategy of (4.1). This means that, if the PV panels are equal, the ones connected to E_1 are half of the panels connected to E_2 and a quarter of the panels connected to E_3 .

Table 4.1 Switching States of the Proposed Basic Unit

S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	V_{out}
1	0	0	0	0	0	1	1	0	0	E_1
0	0	0	0	1	1	1	0	1	0	E_2
1	0	0	0	0	0	0	0	1	1	E_3
0	0	0	0	1	1	1	1	0	0	E_1+E_2
1	0	0	0	0	0	0	1	0	1	E_1+E_3
0	0	0	0	1	1	0	0	1	1	E_2+E_3
0	0	0	0	1	1	0	1	0	1	$E_1+E_2+E_3$
0	1	0	0	0	0	0	0	1	1	$-E_1$
0	0	1	1	0	0	0	1	0	1	$-E_2$
0	1	0	0	0	0	1	1	0	0	$-E_3$
0	0	1	1	0	0	0	0	1	1	$-E_1-E_2$
0	1	0	0	0	0	1	0	1	0	$-E_1-E_3$
0	0	1	1	0	0	1	1	0	0	$-E_2-E_3$
0	0	1	1	0	0	1	0	1	0	$-E_1-E_2-E_3$
1	0	0	0	0	0	1	0	1	0	0

4.3 Operation principle

Table 4.1 shows the switches' operation versus output voltage. For example, when S_1 , T_1 , and T_2 turn on, with the rest of the switches off, the output voltage becomes E_1 , when S_2 , T_1 , and T_2 turn on output voltage becomes $-E_3$, and so on. Switches are controlled in order not to have any conducting diodes that can short-circuit the DC sources. Fig. 4.1.b shows the switching pattern that the controller of the inverter produces using a sinusoidal reference. It shows which of the inputs (E_1 , E_2 or E_3) are selected to have a signal close to a sinusoidal waveform in the output port. The voltage difference between the multilevel output signal and the sinusoidal signal is the source of THD and must be minimized.

Figure 4.2 shows the current path at eight different modes, which are detailed at Table 4.1. The other switching modes can be obtained using Table 4.1. The switches must be switched on and off, avoiding short-circuit in the inputs and following the reference signal. In order to create a sinusoidal waveform, the switching pattern must change according to the control presented in Section 4.3. The transition from one state to the next one is done at the transition angles, $\alpha_1, \alpha_2, \dots, \alpha_N$, which are shown in Figure 4.3 and Table 4.2. Notice that during a whole cycle, which lasts 20ms (50Hz), the converter changes its output 28 times using the 15 levels. The total amount of commutations including all of the switches in one cycle can be extracted using Figure 4.2 and Table 4.1. It gives 100 commutations per cycle including all of the switches, so the switching losses is low.

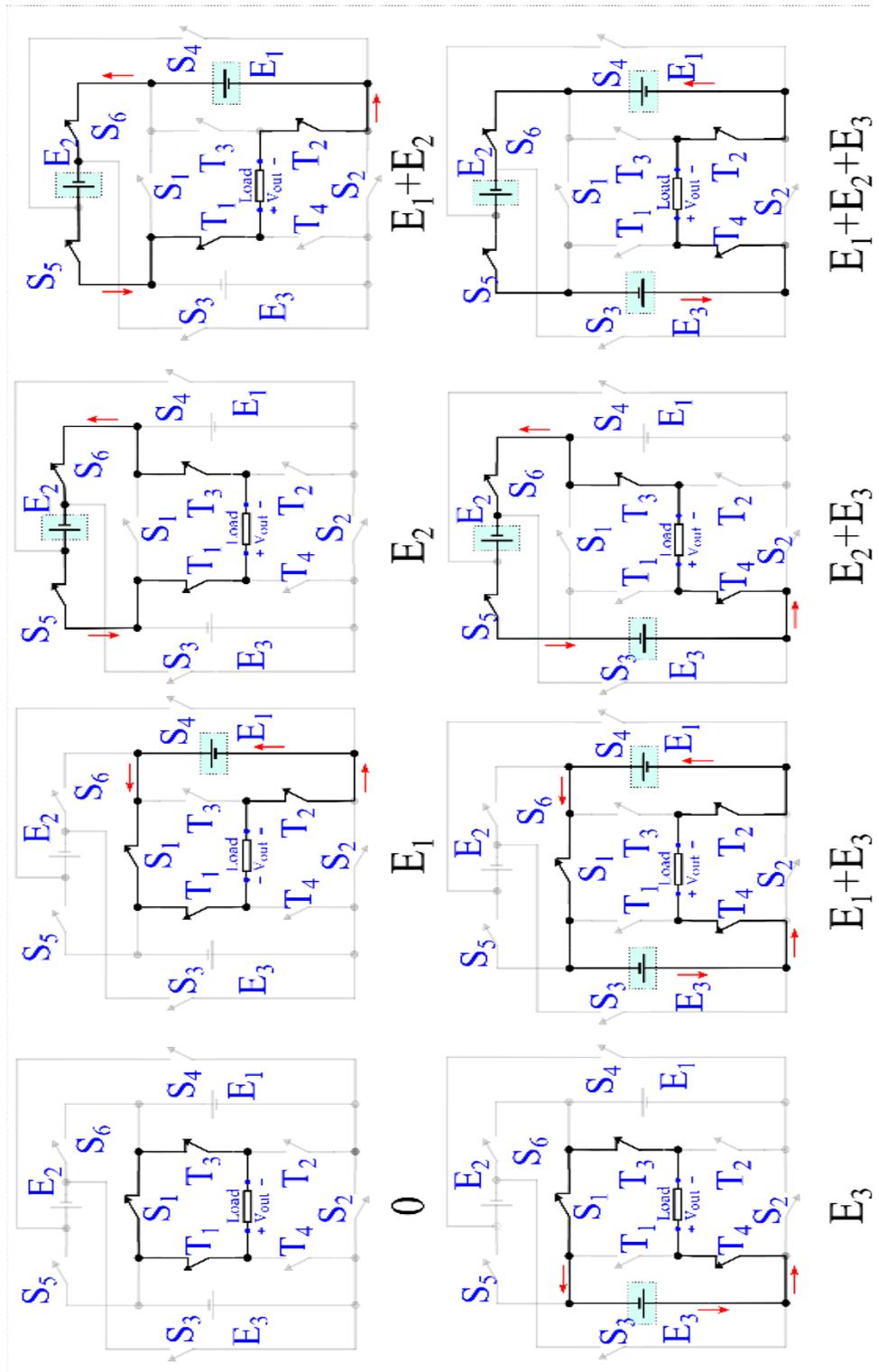


Figure 4.2. Current path and state of switches ($0 < t < T/4$).

Table 4.2 Switching angles ($0 < t < T/2$)

Angle	α_1	α_2	α_3	α_4	α_5	α_6	α_7
α_i	4.09°	12.37°	20.92°	30.00°	40.00°	51.78°	68.21°
$\text{Sin}(\alpha_i)$	0.071	0.214	0.357	0.5	0.642	0.785	0.928
$\text{Cos}(\alpha_i)$	0.997	0.976	0.934	0.866	0.766	0.618	0.371

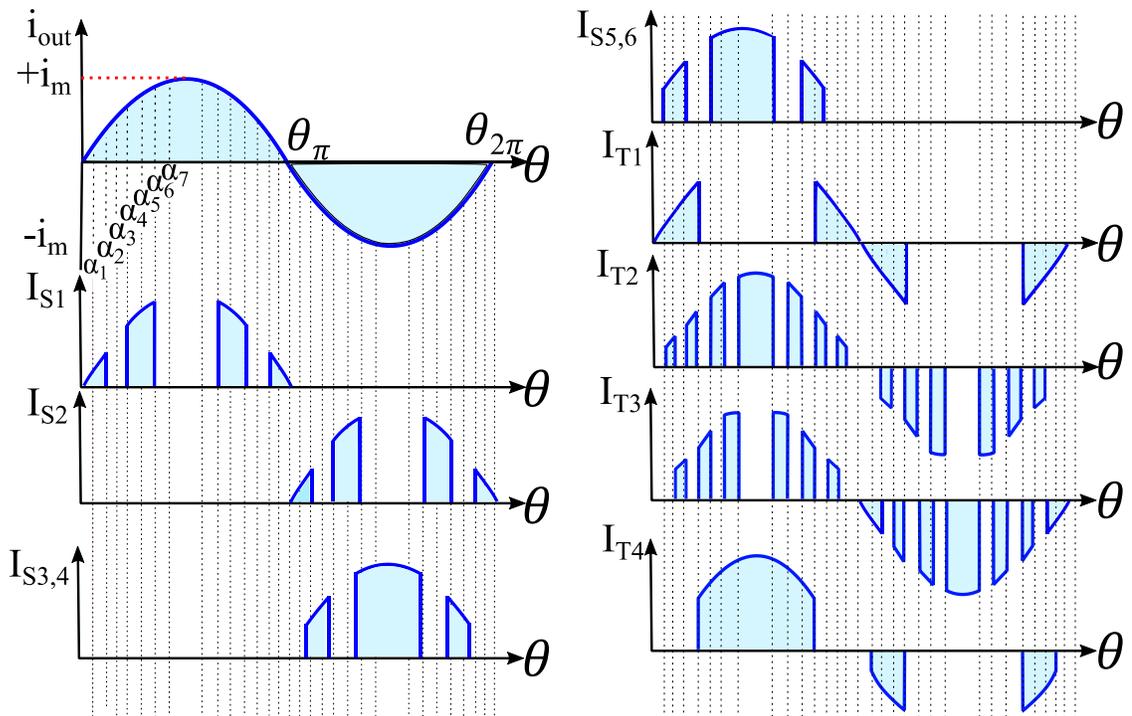


Figure 4.3. Current waveforms through the switches.

4.4 Current through the switches

In order to evaluate power losses and to select the switches, the current through the switches during the on-state must be calculated. Particularly, the average and the RMS current rating are needed. In the proposed multilevel inverter, the waveform of output current can be considered sinusoidal by assuming the high number of levels. The current waveforms through the diodes and switches are depicted in Figure 4.3. By assuming a constant temperature, the average current can be calculated by:

$$I_{ave}(S_n) = \frac{1}{T} \int_0^T i_{(t)} dt. \quad (4.2)$$

For example, the average current for switch S_1 is calculated below:

$$\begin{aligned} I_{ave}(S_1) &= \frac{1}{T} \int_0^T I_{(t)} dt = \frac{2}{2\pi} \left[\int_0^{\alpha_2} I_m \sin\theta d\theta + \int_{\alpha_4}^{\alpha_6} I_m \sin\theta d\theta \right] \\ &= \frac{I_m}{2\pi} \left[-2[\cos\theta|_0^{\alpha_2} + \cos\theta|_{\alpha_4}^{\alpha_6}] \right] = \frac{I_m}{\pi} [1 + \cos\alpha_4 - \cos\alpha_2 - \cos\alpha_6] \end{aligned} \quad (4.3)$$

where α_2 , α_4 and α_6 are the angles of the sinusoidal waveform that start and end a conductive period for S_1 and I_m is the peak of the output current. These angles are shown in Fig. 4.3 and Table 4.2, and correspond to the case of the converter working at the maximum power with the minimum THD. The angles can be obtained by:

$$\alpha_j = \sin^{-1} \left(\frac{2j-1}{2N_{level}} \right), \text{ for } j = 1, \dots, (N_{level} - 1)/2. \quad (4.4)$$

where N_{level} is the number of levels of the output voltage ($N_{level}=15$). For the first quadrant, seven angles exist in the proposed converter. The angles in the other quadrants can be obtained using the symmetric properties of the sinusoidal signal.

The average current is computed only in the first quarter of the period and is multiplied by two due to the signal symmetry. The value of I_m can be obtained by:

$$I_m = \frac{V_{o_{max}}}{\sqrt{R_L^2 + X_L^2}} = \frac{V_{o_{max}}}{|Z_L|} \quad (4.5)$$

where R_L, X_L are resistance and reactance of the load, respectively. $V_{o_{max}}$ is the peak of the output voltage.

Figure 4.4 shows the current rating of the switches normalized with the output RMS current. For example, for the average current of S1, using (4.3), the rating is:

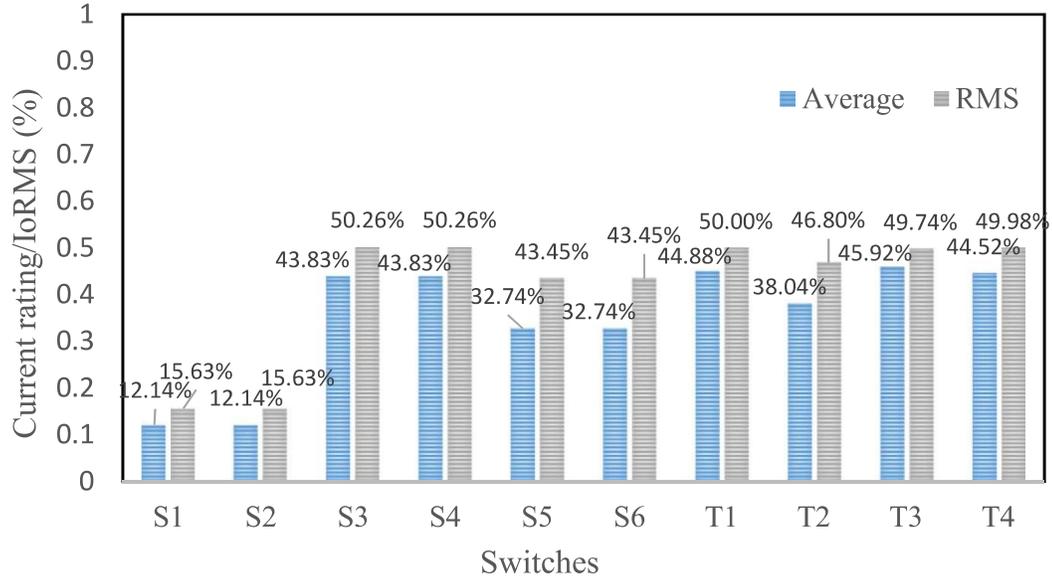


Figure 4.4 Current rating for the switches in the proposed structure normalized with the output RMS current.

$$\frac{I_{ave}(S_1)}{I_{rms}(output)} = \frac{I_{ave}(S_1)}{I_m(output)/\sqrt{2}} = 12.14\% \quad (4.6)$$

The RMS current for each of the switches:

$$I_{RMS}(S_n) = \sqrt{\frac{1}{T} \int_0^T i_{(t)}^2 dt}. \quad (4.7)$$

Similarly, to the average current, the RMS was calculated and normalized for every switch, as shown in Figure 4.4. As the ratings are different for each switch, it is possible to select the switch according to these values to optimize cost, power rating and thermal design for implementing the prototype. According to Figure 4.4, the switches can be divided into two categories. $S_3, S_4, S_5, S_6, T_1, T_2, T_3,$ and T_4 have an average current around 40% of the output RMS current, and S_1 and S_2 switches have only around 10% of the output RMS current.

4.5 Calculation of power losses

As in any other converter, semiconductor power losses can be divided in conduction and switching losses. Conduction losses occur when the switch is on and depend on the current through the switches. Switching losses exist during turn-on and turn-off transitions and they are proportional to the switching frequency. For this particular modulation the switching frequency is very low, so switching losses are extremely low, which is very favorable for high power applications.

Bidirectional switches can be done in different ways. Figure 4.5.a shows a diode bridge with a single switch that is able to control current in both directions. This switch topology consists of four ultra-fast diodes with a controllable unidirectional switch. The advantage of this switch is that it has a simple construction and requires only one switch, for example, one insulated-gate bipolar transistor (IGBT), and the blocking voltage is shared between two diodes and one IGBT. However, the conduction losses are due to two voltage drops in the diodes and one IGBT saturation voltage.

A structure which reduces the voltage drop is shown in Figure 5.5.b. This structure has only two IGBTs, so only one saturation voltage and one forward voltage

drop in the diode. Therefore, this structure has reduced conduction losses. Besides, the two IGBTs can be triggered using the same driver; this means that to have a bidirectional switch instead of a unidirectional switch does not add complexity in the driver and control stages, so the cost is not increased. The first topology was used for calculating the losses in the following section thus it imposes a maximum limit on power losses; other configurations will reduce the power losses and can be easily calculated following the same approach.

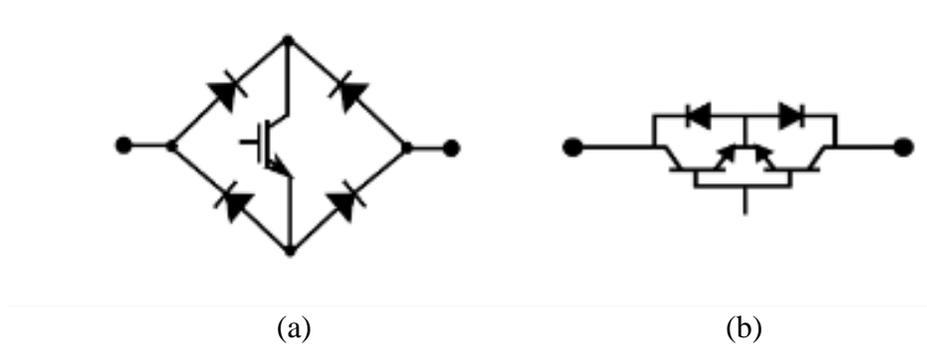


Figure 4.5 Bidirectional switches: (a) Bridge of diodes with single IGBT, (b) Double IGBT structure.

4.5.1 Conduction Losses

Conduction losses can be calculated using the on-voltage drop in the switch:

$$P_{\text{Cond}} = \frac{1}{T} \int_{t+T}^T V_{\text{on}}(t) \cdot I(t) dt = \frac{V_{\text{SAT}}}{T} \int_{t+T}^T |i(t)| dt + \frac{r_{\text{on}}}{T} \int_{t+T}^T i^2(t) dt = V_{\text{SAT}} I_{\text{AVEABS}} + r_{\text{on}} I_{\text{RMS}}^2 \quad (4.8)$$

where $V_{\text{on}}(t)$ is the on-voltage drop, $i(t)$ is the current through the switch and r_{on} is the on-resistance. In bidirectional switches, $V_{\text{on}}(t)$ has the same sign as the current through the switch, so the average absolute current must be used, I_{AVEABS} . The total conducting losses is the sum of the losses in each switch. Thus, using (4.8) and switching intervals of section 4.5.2, the total conducting losses are:

$$P_{cond}(Total) = \sum_{i=1}^{10} P_{Con}(Si) = (0.459)(V_T + 2V_D) I_m + (5.87 \cdot 10^{-3})(R_T + 2R_D) \frac{I_m^2}{2}, \quad (4.9)$$

where V_T and R_T are the saturation voltage and on-resistance of the IGBT, V_D and R_D are the forward voltage drop and on-resistance of one diode. Moreover, $5.87 \cdot 10^{-3}$ is the cofactor for power loss of R_T and R_D in the proposed topology. The losses per switch are illustrated in Figure 4.6.a as the percentage of the total conductive losses. It can be seen that the S_3 , S_4 , S_5 , S_6 , T_1 , T_2 , T_3 , and T_4 switches dissipate 94% of conduction losses.

4.5.2 Switching Losses

The switching losses are the energy losses during the transition (from on to off and vice versa) multiplied by the switching frequency. In order to estimate the energy losses, the current and voltage profiles can be linearized during the transition [22]. Thus, the energy losses for the on-transition and off-transition:

$$E_{on} = \int_0^{t_{on}} v(t)i(t) dt = \frac{V_{switch} I t_{on}}{2}, \quad (4.10)$$

$$E_{off} = \int_0^{t_{off}} v(t)i(t) dt = \frac{V_{switch} I t_{off}}{2}, \quad (4.11)$$

where t_{on} and t_{off} are the duration of the switching transition, $v(t)$ and $i(t)$ are the voltage and current during the transition. I is current through the switch at the beginning of the off-transition and at the end of the on-transition, and V_{switch} is the voltage across the switch at the beginning of the on-transition and at the end of the off-transition. Following the same approach as in conducting losses, the total switching losses are:

$$P_{sw}(Total) = \frac{1}{T} \left[\sum_{i=1}^{10} (E_{off(S_i)} + E_{on(S_i)}) \right] = (25.1) E_1 \frac{\Delta t}{T} I_m. \quad (4.12)$$

where it is considered that $t_{off}=t_{on}$. The distribution of total switching losses is illustrated in Figure 4.6.b.

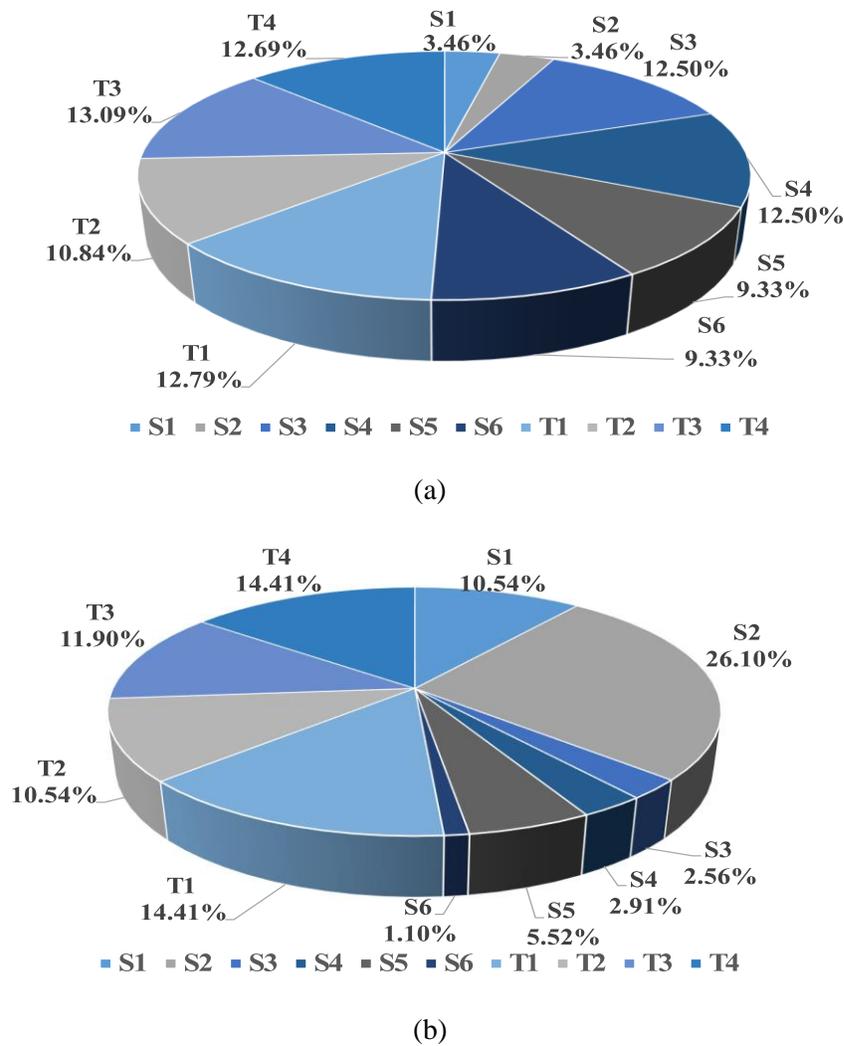


Figure 4.6 Losses of switches in the proposed structure, (a) Conductive losses. (b) Switching losses.

Finally, based on conducting and switching losses, the efficiency can be calculated as:

$$\eta_{eff} = \frac{P_{out}}{P_{in}} = \frac{1}{1 + \frac{P_{con}(Total) + P_{sw}(Total)}{P_{out}}} \quad (4.13)$$

Where

$$P_{out} = \frac{7E_1 I_m}{2} = 3.5E_1 I_m, \quad (4.14)$$

for the maximum power and voltage. The efficiency is:

$$\eta_{eff} = \frac{1}{1 + (7.17)\Delta t/T + (0.1311/E_1)(V_T + 2V_D) + (0.00838/E_1)(R_T + 2R_D) I_m}, \quad (4.15)$$

For example, $E_1=50V$, which means a maximum output voltage of 350V and $I_m=100A$, considering $\Delta t=1\mu s$, $T=20ms$, and $V_T+2V_D=3.5V$ $R_T+2R_D=90m\Omega$, the maximum efficiency is 99%, and the conduction losses are dominant. Improving the switches can produce even better efficiency.

4.6 Simulation results

The following parameters are considered to calculate the efficiency of the proposed module: $V_T = 1.5V$, $V_D = 1V$, $R_T=0.033\Omega$, $R_D=0.06\Omega$, $t_{on} = t_{off} = \Delta t = 1\mu s$, $V_{orms} = 59V$, $P_{out}=65W$ and $f = 50Hz$, $E_1 = 12V$. The load is series $RL = 48\Omega + 125 \mu H$. These parameters were selected in order to compare with the experimental results. The basic unit (Figure 4.1.a) was simulated in MATLAB/Simulink. The converter's output voltage is a sinusoidal signal at 50 Hz. This converter has 28 transitions in each period (20ms), as shown in Figure 4.1.b. The simulated efficiency is 94.2%, which matches the theoretical calculations.

The THD is defined as:

$$THD = \frac{\sqrt{\sum_{h=2,3,4,5,\dots}^{\infty} V_{oh}^2}}{V_{o1}} = \sqrt{\left(\frac{V_{o,rms}}{V_{o1}}\right)^2 - 1}, \quad (4.16)$$

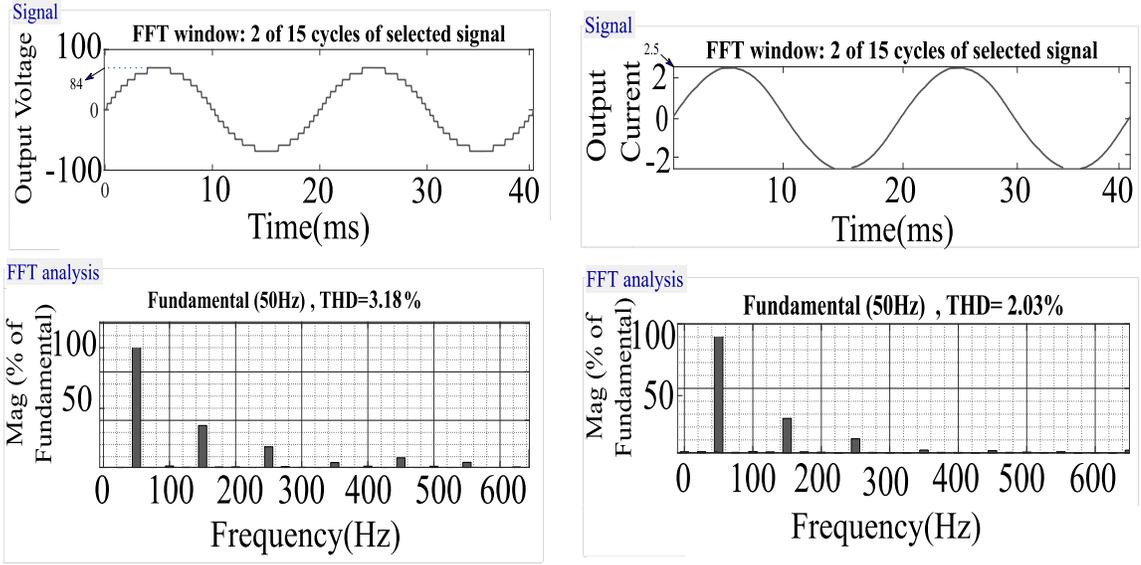


Figure 4.7 Simulation results (a) Output voltage. (b) Output current.

where h is the harmonic order, $h = 1$ corresponds to the main frequency. As the waveform is completely symmetric, the even harmonics are zero. V_{oh} and V_{o1} are the h th-order harmonic and fundamental harmonic RMS values of the output voltage waveform. Furthermore, V_{orms} is the total RMS value of the output voltage. V_{o1} and $V_{o,rms}$ can be calculated using:

$$V_{o,rms}^2 = \frac{4E1^2}{2\pi} \left(-\alpha_1 - 3\alpha_2 - 5\alpha_3 - \dots - (2n-1)\alpha_n - (2N_{level}-1)\alpha_{\frac{N_{level}-1}{2}} + \left(\frac{N_{level}-1}{2}\right)^2 \frac{\pi}{2} \right) \quad (4.17)$$

and, if the number of levels is large, the first harmonic can be estimated as:

$$V_{o1} = \left(\frac{N_{level}-1}{2}\right) \frac{E1}{\sqrt{2}} \quad (4.18)$$

By considering (4.16) -(4.18), it is observed that the THD value depends on the switching angles and the number of levels. It is clear that if the number of levels is

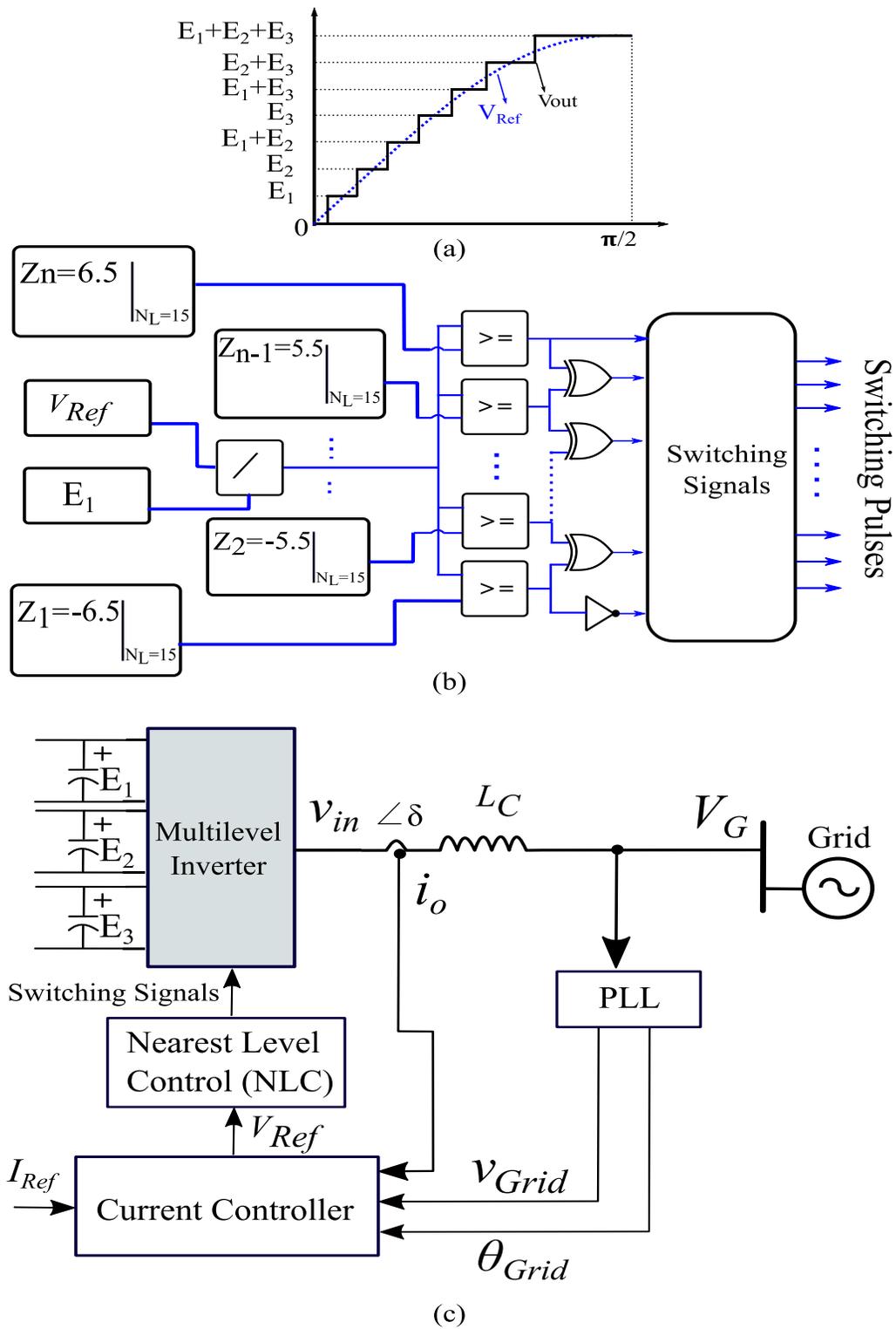


Figure 4.8 Nearest level control (NLC) with (a) sampled reference voltage and (b) simplified NLC implementation (c) Control block diagram of the grid-connected inverter.

increased, the output waveform will be similar to a sinusoidal waveform, and the THD value will decrease. Figure 4.7 shows the simulation results for output voltage and current with the proposed structure. The THD value for voltage and current is 3.18% and 2.03%. The THD of the current is slightly lower than the THD of the voltage because the R-L load acts as a filter.

4.7 Control Modulation Method

Several modulation techniques have been analyzed and applied to multilevel converters, such as Carrier-Based (CB) PWM, Selective Harmonic Elimination (SHE) PWM, and Space Vector (SV) PWM. CBPWM needs various carrier signals to achieve gate pulses and causes higher switching losses. In SVPWM, the algorithm's complexity will increase as the number of levels at the output rises. Likewise, using SHEPWM, the estimation of switching angles becomes very complex as the number of levels increases [22-24].

The nearest level control (NLC) is a low switching frequency PWM method [25], where the calculation time is reduced. So, it is a simple control algorithm attractive for a high number of levels.

The nearest output voltage level, v_{level_n} can be determined as:

$$v_{level_n} = round(v_{ref}/E_1), \quad (4.19)$$

where v_{ref} is the reference voltage and E_1 is the lowest level, and (4.19) gives the nearest integer. Figure 4.8 shows the scheme of a simplified NLC implementation. The level is chosen in order to be as close as possible to the reference signal (Figure 4.8.a).

Figure 4.8.b shows the control diagram in order to select the proper level, where

$$z_n = n - 7.5 \text{ for } n = [1, 2, \dots, (N_L - 1)]. \quad (4.20)$$

The reference signal, $v_{ref} = V \sin(\omega t)$, is divided by E_1 , and then after many comparisons, the proper level is selected.

4.8 Cascading of the proposed structure

In order to reach higher voltages, increase the power rating, as well as the number of voltage levels, and decrease the voltage stress on power semiconductors in multilevel inverters, a cascaded structure is proposed. The cascading technique is useful in photovoltaic and grid-tied systems due to the PV energy system’s capability of synthesizing stepped AC output voltage from several DC sources. However, due to the unequal DC inputs, the complexity of control increases, particularly for solar application including partial shaded conditions.

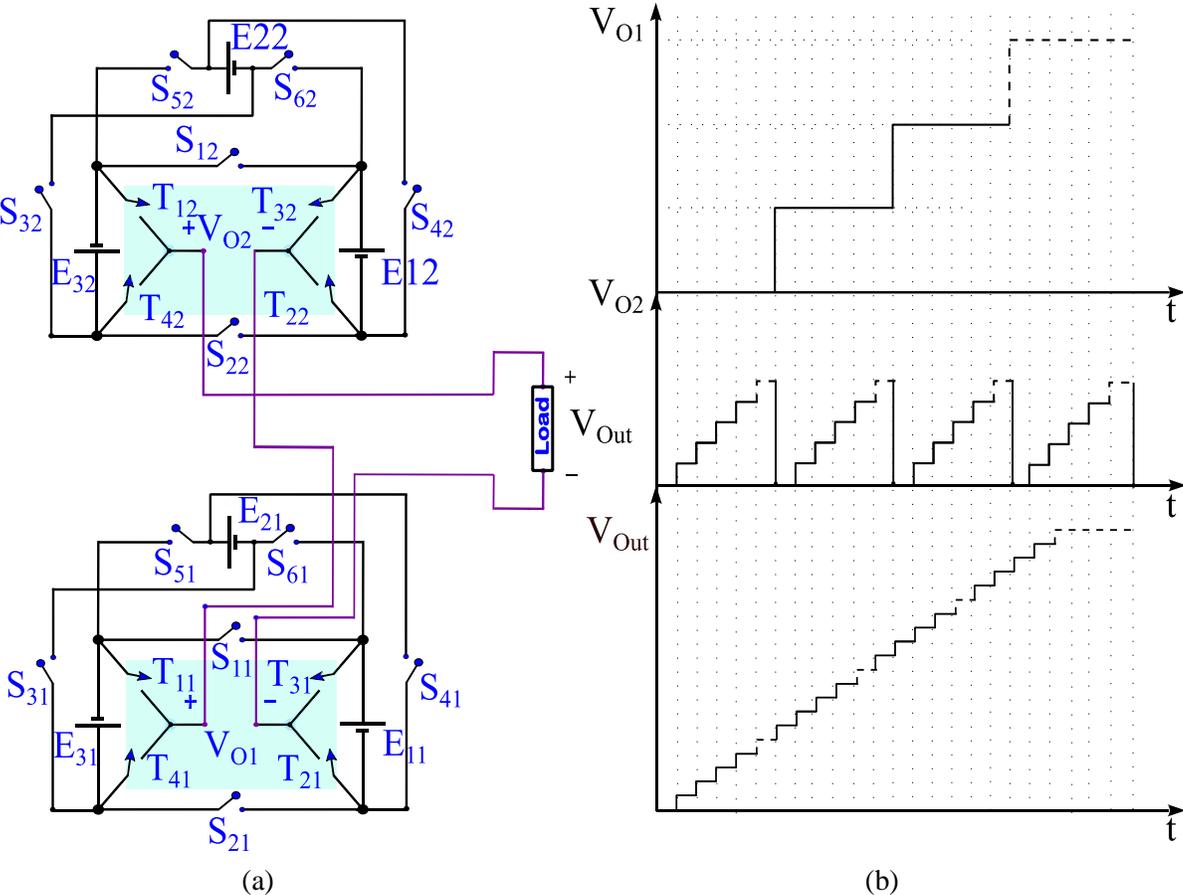


Figure 4.9 Cascading of proposed structure (a) Cascaded structure with two stages of the proposed topology. (b) Output voltage for each stage and total output voltage.

Table 4.3 Output Voltage of Proposed Cascade Multilevel Converter Topology ($0 < t < \pi/2$).

State	Switching pattern	Output voltage
1	$S_{11}, T_{11}, T_{31}, S_{12}, T_{12}, T_{32}$	0
2	S_{11}, T_{11}, T_{21}	E_{11}
3	$S_{51}, S_{61}, T_{11}, T_{31}$	E_{21}
4	$S_{51}, S_{61}, T_{11}, T_{21}$	$E_{11}+E_{21}$
5	S_{11}, T_{31}, T_{41}	E_{31}
6	S_{11}, T_{21}, T_{41}	$E_{31}+E_{11}$
7	$S_{51}, S_{61}, T_{11}, T_{21}$	$E_{31}+E_{21}$
8	$S_{51}, S_{61}, T_{11}, T_{41}$	$E_{11}+E_{21}+E_{31}$
9	$S_{11}, T_{11}, T_{21}, S_{12}, T_{12}, T_{32}$	$E_{12}+E_{11}$
.	.	.
.	.	.
.	.	.
62	$S_{51}, S_{61}, T_{21}, T_{41}, S_{52}, S_{62}, T_{32}, T_{42}$	$E_{12}+E_{13}+ E_{32}+E_{22}+E_{12}$
63	$S_{51}, S_{61}, T_{11}, T_{41}, S_{52}, S_{62}, T_{12}, T_{42}$	$E_{11}+E_{21}+E_{31}+ E_{12}+E_{22}+E_{32}$

Figure 4.9.a shows the proposed cascaded structure with two stages. Figure 5.9.b shows part of the output voltage for each stage (V_{O1}, V_{O2}) and the total output voltage (V_{Out}). The cascaded structure's switching pattern, which has 63 states to produce a positive cycle, is shown in Table 4.3. In a cascaded structure, every basic unit's switch pattern is different from each other because it has a different value in its output voltage. Moreover, Table 4.3 shows the output voltage as a function of the switching state. The output voltage of the cascaded structure is the sum of every unit stage. Thus,

$$V_{out} = V_{O1} + V_{O2} + \dots + V_{ON} \quad (4.21)$$

where $V_{O1}, V_{O2}, \dots, V_{ON}$ are the output voltages of every single unit connected in series. The maximum output voltage is:

$$V_{o,max} = E_{11} + E_{21} + E_{31} + E_{12} \dots + E_{3N} \quad (4.22)$$

where the first index is the DC source in each stage (1,2 and 3) and the second index is the number of stages from 1 to N. Two algorithms are described for determining the values of the cascaded structure DC input sources.

Algorithm 1: Equal DC input sources

In this algorithm, the values of DC sources in each unit are the same:

$$E_{1i} = E_{2i} = E_{3i} = Vdc. \quad (4.23)$$

The number of output voltage levels, including positive, negative, and zero states are:

$$N_{\text{Levels}} = 6i + 1 \quad i = 2, 3, 4, \dots, N \quad (4.24)$$

where i is the number of stages. The maximum amplitude of the output voltage is:

$$V_{o,max} = 3iVdc \quad i = 2, 3, 4, \dots, N \quad (4.25)$$

Using this algorithm, there are many independent DC sources, but all of them have the same output voltage, which reduces the complexity of the auxiliary DC side.

Algorithm 2: Non-equal DC input sources

The DC sources of each basic unit are non-equal in the second algorithm. For the first unit, the DC sources are determined as follows (1):

$$E_{11} = Vdc \quad E_{21} = 2E_{11} \quad , \quad E_{31} = 2E_{21}, \quad (4.26)$$

for the second stage

$$E_{12} = \frac{E_{11}}{8} \quad , \quad E_{22} = 2E_{12} \quad , \quad E_{32} = 2E_{22}. \quad (4.27)$$

This algorithm extracts all the advantages of the basic unit presented in Section 4.2.

Moreover, if the structure has more than two stages, for k-th stage

$$E_{1k} = \frac{E_{1(k-1)}}{8} \quad , \quad E_{2k} = 2E_{1k} \quad , \quad E_{3k} = 2E_{2k} . \quad (5.28)$$

The number of output voltage levels can be calculated as follows:

$$N_{\text{Levels}(i)} = 2 \left[8 \left(\frac{N_{\text{Levels}(i-1)} - 1}{2} \right) + 7 \right] + 1 \quad (4.29)$$

$i = 2, 3, 4, \dots, k$ is the number of stages,

where $N_{\text{Levels}(1)} = 15$. For example, to determine the output voltage levels of two stages in the cascaded structure, we have:

$$i = 2, \quad N_{\text{Levels}(1)} = 15 \rightarrow N_{\text{Levels}(2)} = 127 \text{ levels}. \quad (4.30)$$

The maximum output voltage is

$$V_{o,max} = \left(\frac{N_{\text{Levels}(i)} - 1}{2} \right) V_{dc}. \quad i = 2, 3, 4, \dots, k. \quad (4.31)$$

These two algorithms have some advantages and drawbacks. In the equal input sources algorithm, switching losses are low because the number of transitions within a period are reduced about 20 times for the two stage case compared to the non-equal sources algorithm (28 transitions vs. 255 transitions). However, the non-equal case transitions occur at different voltages, so some units have higher switching losses than others due to the differences in the input DC sources. To conclude the 2nd algorithm has much more levels, so much lower THD, with slightly more un-equally distributed switching losses, and much higher complexity in the input DC side in order to produce more different DC levels. According to the application and the available inputs, the proper algorithm must be chosen, reminding that the dominant losses are the conducting losses.

4.9 Comparison of proposed structure with other topologies

The proposed cascaded multilevel inverter is compared with several cascaded multilevel inverters that have been presented in the literature. Table 4.3 compares the number of switches, diodes, DC voltage sources (or DC links), and TSV, which

Table 4.4 Comparison of several cascaded multilevel topologies (N_L = Number of levels)

	NUMBER OF SWITCHES	NUMBER OF DIODES	Number of DC links / sources	TSV*xVdc
CHB	$2(N_L - 1)$	$2(N_L - 1)$	$(N_L - 1)/2$	$2(N_L - 1)$
NCML[9]	$N_L + 3$	$N_L + 3$	$(N_L - 1)/2$	$3(N_L - 1)$
2CLHB[10]	$N_L + 1$	$N_L + 1$	$(N_L - 1)$	$2(N_L - 1)$
CSMLI[11]	$N_L + 1$	$N_L + 1$	$(N_L - 1)/2$	$2(N_L - 1)$
K-Type[17]	$14 \left(\frac{N_L - 2}{12} + 1 \right)$	$14 \left(\frac{N_L - 2}{12} + 1 \right)$	$2 \left(\frac{N_L - 2}{12} + 1 \right)$	$32 \left(\frac{N_L - 2}{12} + 1 \right)$
ST-Type[27]	$12 \log_{17} N_L$	$12 \log_{17} N_L$	$4 \log_{17} N_L$	$5 \left(\frac{N_L - 1}{2} \right)$
Novel H-Bridge [14]	$2 \log_2 N_L + 1$	$2 \log_2 N_L + 1$	$\log_2 \left(\frac{N_L + 1}{2} \right)$	$2(N_L - 1)$
Proposed Structure using Fig. 5.a	$3 \log_2 N_L$	$12 \log_2 N_L$	$\frac{9}{10} \log_2 N_L$	$17(N_L - 1)/20$

indicates the maximum blocking voltage across each semiconductor device. The second algorithm presented in Section 4.8 was used for comparison.

Table 4.4 includes the conventional cascaded H-bridge converter (CHB), multilevel DC links (NCML) [9], two capacitor links H-bridge (2CLHB) [10], crossing switch multilevel inverter (CSMLI) [11], Novel H-Bridge[14], K-Type[17], and square T-Type topology (ST-Type) inverter presented in [27]. The number of switches, the number of DC links and TSV are reduced down to $3 \log_2 N_L$, $\frac{9}{10} \log_2 N_L$ and $17(N_L - 1)/20$ respectively, for the proposed structure. On the other hand, in the proposed structure, the number of diodes is more than other topologies because a bridge of diodes with a single IGBT has been used as a bidirectional switch (Figure 4.5.a).

Figure 4.10.a compares the number of DC voltage sources in the proposed topology with other cascaded multilevel inverters, in terms of the number of levels. It shows that the proposed cascaded inverter needs a lower number of DC voltage sources than CHB, 2CLHB [10], and CMSLI [11] (which have the same number) and the ACML[13], K-Type [17] and ST-Type [27]. The number of DC voltage sources is similar in the proposed topology, NGCML [31], and novel H-Bridge [14]. This comparison shows that the proposed converter has a low number of isolated DC inputs.

Figure 4.10.b compares the number of switches in the proposed topology with other cascaded multilevel inverters. It is clear that the proposed topology requires lower

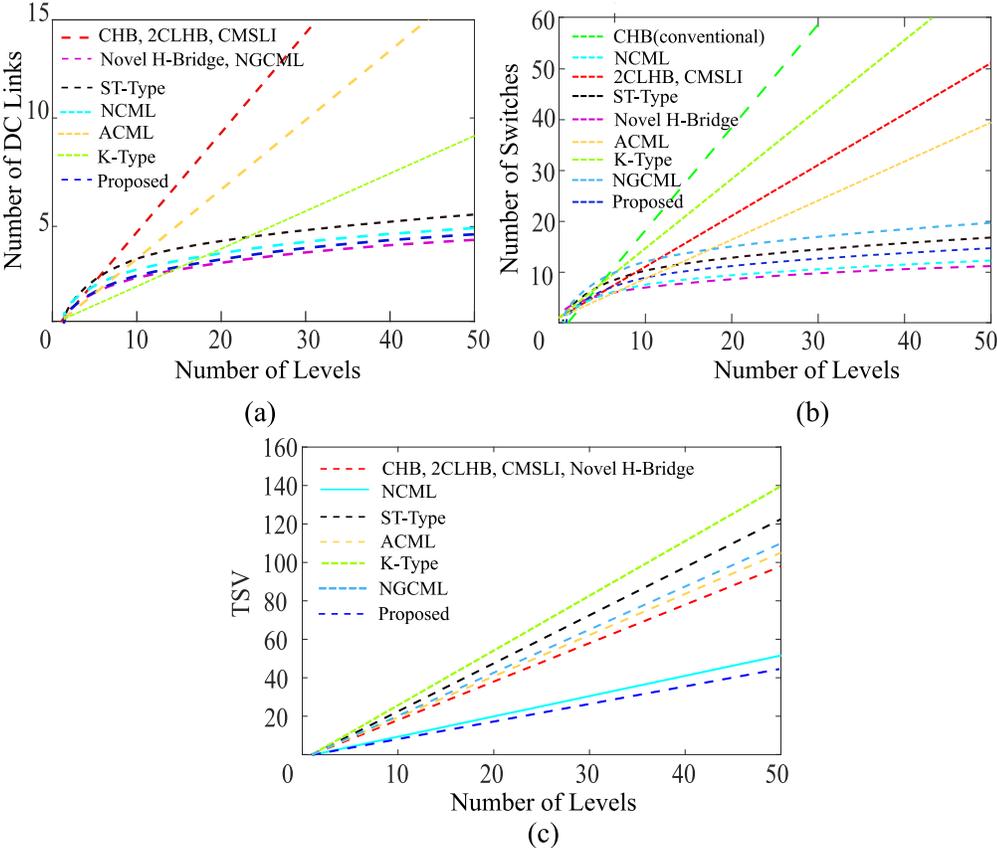


Figure 4.10 Comparative studies: The number of (a) DC links, (b) switches, and (c) TSV in terms of the number of levels. number of switches compared with most of the mentioned topologies, except for Novel H-Bridge and NCML. In Figure 4.10.c, it can be seen that the proposed structure

has the lowest TSV compared to other references. Table 4.5 shows a comparison of several multilevel topologies. It can be seen that the proposed topology has reasonable characteristics. However, to have more accurate comparison needs to consider same conditions (Inputs, components, and control methods) for all topologies.

Table 4.5 Comparison of several multilevel topologies (Low(L), Medium(M), High(H))

	METHOD OF CONTROL	THD	Efficiency	TSV	Losses
NCML[9]	FUNDAMENTAL FREQUENCY SWITCHING	M	M	H	M
2CLHB[10]	PWM	L	M	L	M
CSMLI[11]	FUNDAMENTAL FREQUENCY SWITCHING	M	H	L	L
ST-Type[27]	NEAREST LEVEL CONTROL	L	H	H	L
K-Type[17]	NEAREST LEVEL CONTROL	M	H	H	L
ACML[13]	SELECTIVE HARMONIC ELIMINATION	L	M	H	M
Novel H-Bridge [14]	PWM	L	M	L	M
NGCML[31]	SPWM	H	M	H	M
Proposed Structure using Fig. 6.a	NEAREST LEVEL CONTROL	L	M	L	M

4.10 Experimental Results

Experiments on a real prototype, based in Figure 5.1.a, were conducted. Figure 5.11.c shows the prototype, and Table 4.6 lists the converter's main components. The prototype has three parts: the first one is the control part, which is based on the Atmel SAM3X8E ARM Cortex-M3 microcontroller. In this controller, Table 5.1 is used for

Table 4.6 Experimental components

Components	Type
Power Stage	Proposed Inverter
Voltage source(DC)	12, 24, 48 V
Diode	RURP860
IGBT	FGH40N60SFDTU
Capacitor	T491C225M035AT
Load	Variable resistor from R=[24-84]Ohm, L=[200-1000] μ H
Gate drive	HCPL3120

programming and generating the signals to trigger the switches in order to obtain a sinewave in the output. The second part is the driver stage, which includes isolation and negative bias. The last part is the power section, containing the proposed structure to convert DC voltage sources to AC voltage on the load. This part needs isolated DC inputs.

The optimal methods to generate DC inputs are isolated DC/DC converters and multi tap transformer [19], [28-30]. Fig. 4.11.a shows how to provide DC sources using a multi-winding transformer and rectifying units; so only one source is needed, and Figure 4.11.b shows a similar approach using DC/DC converters, where multiple sources can be connected. Figure 4.11.c shows the prototype, and Table 4.6 lists the converter's main components. The prototype has three parts: the first one is the control part, which is based on the AtmelSAM3X8E ARM Cortex-M3 microcontroller. In this controller, Table 4.1 is used for programming and generating the signals to trigger the switches in order to obtain a sine wave in the output. The second part is the driver stage, which includes isolation and negative bias. The last part is the power section, containing the proposed structure to convert DC voltage sources to AC voltage on the load. This part needs isolated DC inputs.

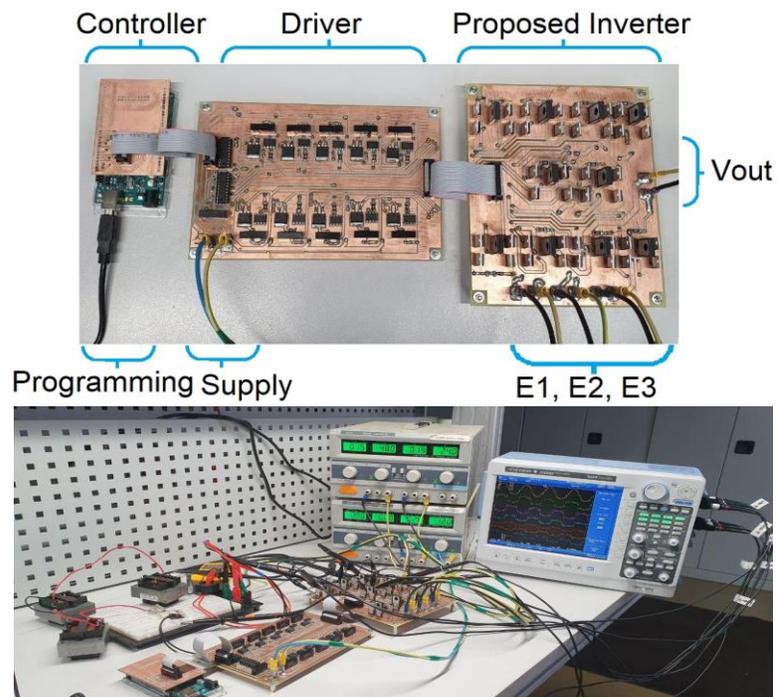
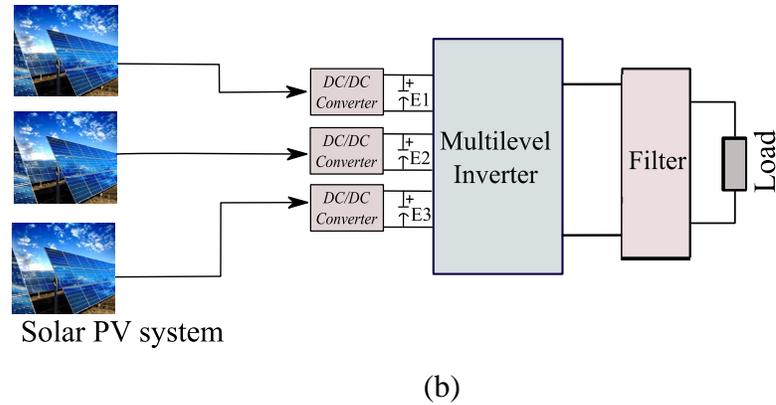
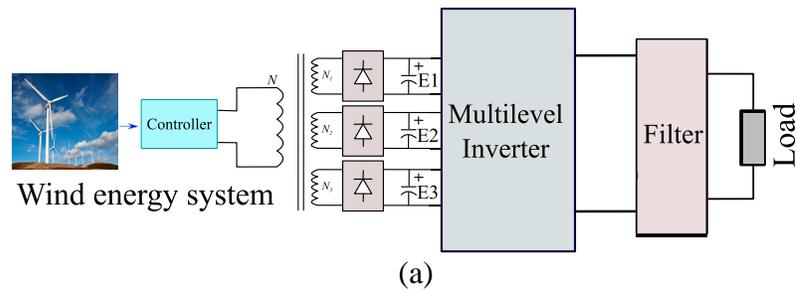


Figure 4.11 Hardware to create multiple DC sources (a) Multi tap transformer, (b) DC/DC converters [19], [28], (c) Prototype of the proposed structure.

Figure 4.12 shows the experimental results for output voltage and current. There are some voltage spikes during the switching processes due to the switches' dead time; during a small time interval, bidirectional switches are off, so the current flows through a snubber circuit. The magnitude of the peaks depends on the amplitude of the load current and the snubber design. Due to the voltage drop on switches, the maximum output voltage is close to 80V instead of 84V. In the experiments, the voltage spikes induce some noise in the current probe as well, which is not present in the circuit.

Figure 4.13 shows the voltages on the S1, S2, S3, S4, S5, and S6 switches. Based on Figure 4.13, it is possible to calculate the voltage stress on each switch. For example, in Figure 4.13.a and 4.13.d, the voltage stresses for S1 and S4 are 84V and 36V.

Figure 4.14.a shows the measured efficiency versus output power at different loads. When the output power increases, the efficiency decreases mainly due to the conduction losses.

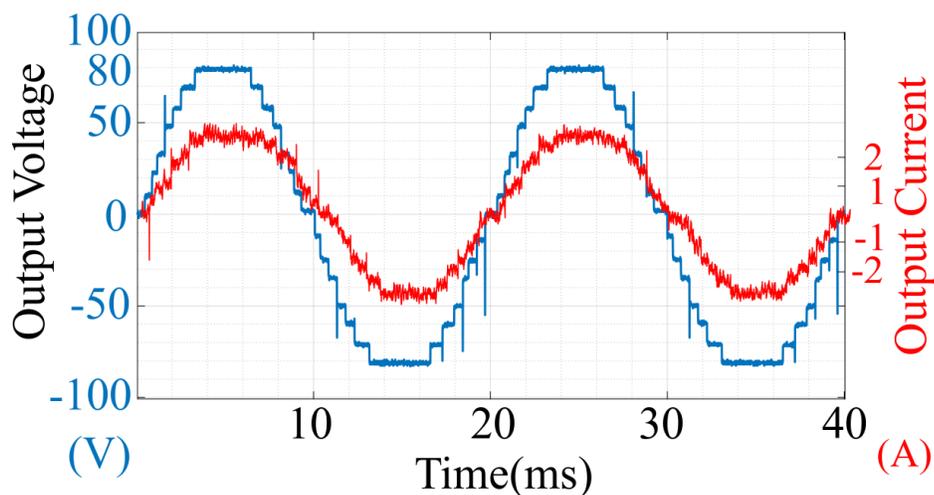


Figure 4.12 Experimental results: Output voltage (blue) and Output current (red)

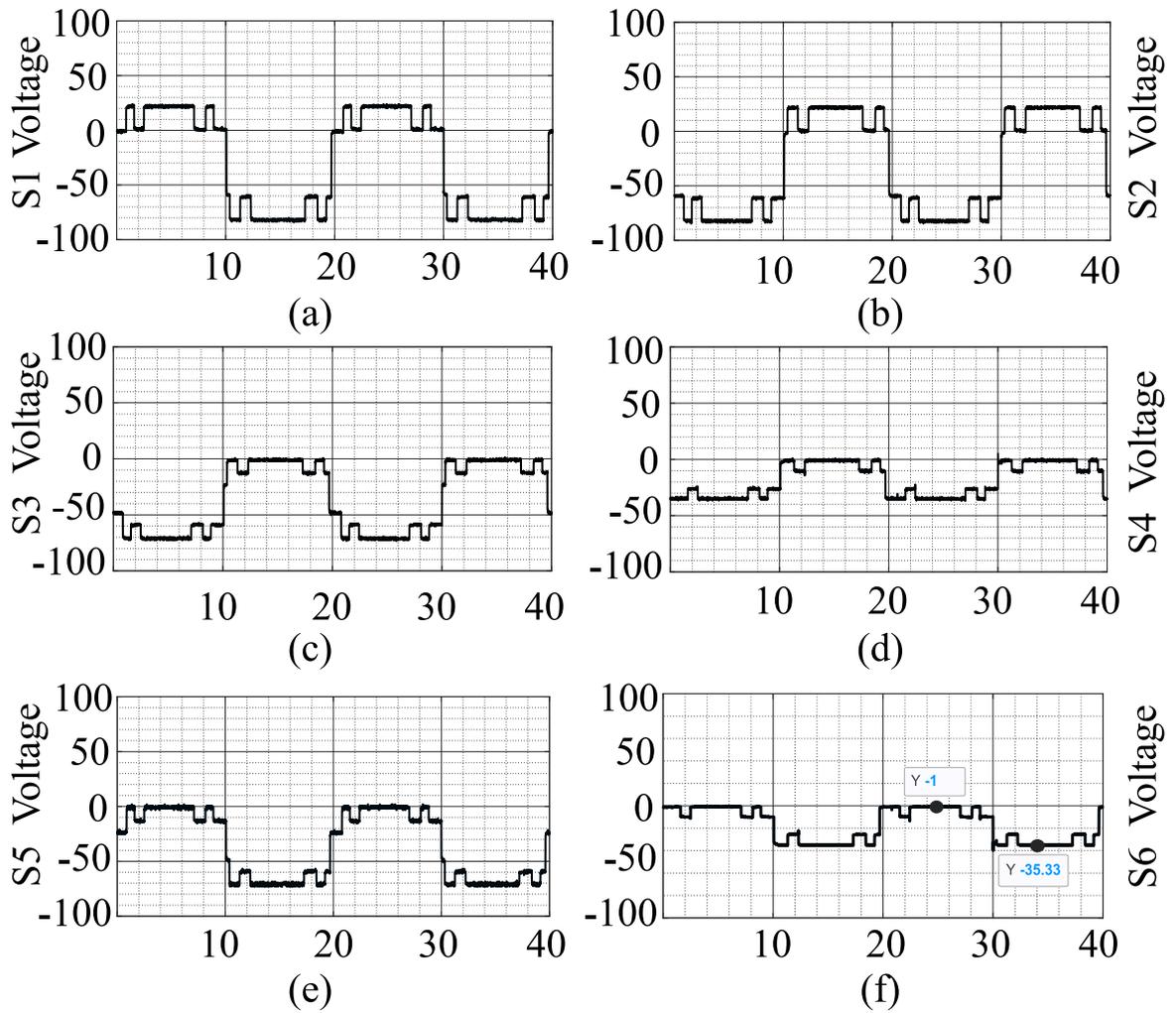
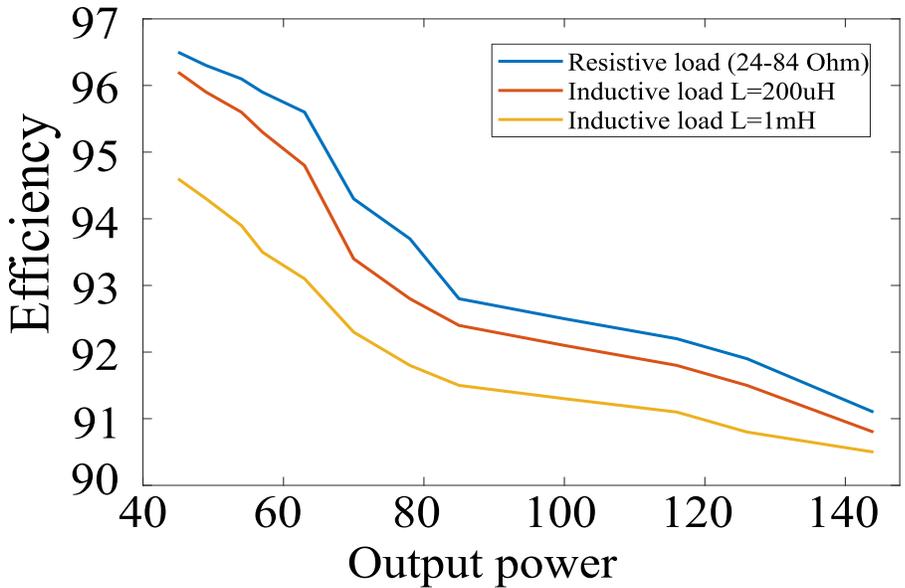


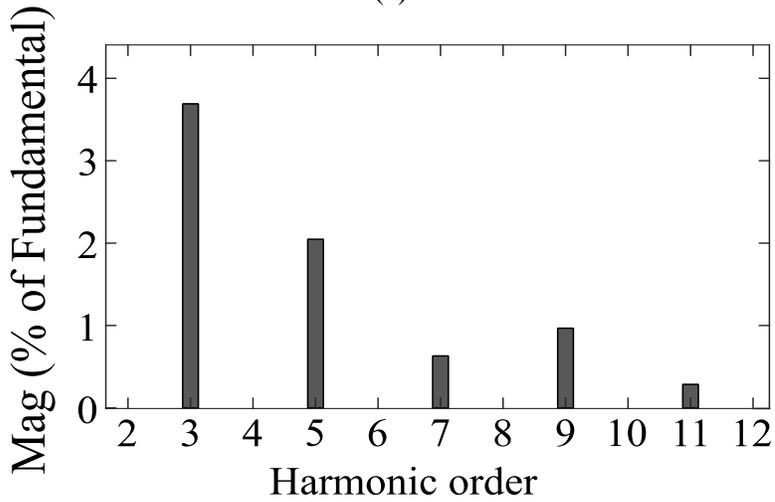
Figure 4.13 Experimental results: voltage on (a) S1, (b) S2, (c) S3, (d) S4, (e) S5, and (f) S6 switches.

Figure 4.14.b shows the FFT of the measured output voltage. It can be seen that the output voltage contains many harmonics but low in magnitude. The results correspond to the maximum power for the load in Table 4.6. Both efficiency and THD are in concordance with the theoretical analysis and simulation results. The theoretical analysis predicts an efficiency of 94%, while experimental results show 93.8% at 65W. The simulated THD was 3.18% for the output voltage at maximum power, while in the prototype, it was 4.5%. The difference can be attributed to the switches' dead

times. For higher voltage applications, efficiency can be much higher because the voltage drops in the diodes and switches do not increase with the output voltage, so the ratio between voltage drops in switches and the output signal is reduced and efficiency increases.



(a)



(b)

Figure 4.14 Experimental results: (a) Measured efficiency against output power at different loads, (b) Measured FFT of the output voltage

4.11 Conclusion

A new topology for multilevel inverter was described in this chapter for renewable energy sources and industrial loads applications. The basic unit of the proposed topology can generate 15 levels with a reduced number of components and three DC inputs. The low number of components leads to a reduction in size, a simple control strategy, and high efficiency. The conduction and switching losses of the proposed 15-level inverter operating under the nearest level modulation technique were determined theoretically.

From this chapter, it suggests a cascade connection of basic units leads to achieving more output voltage levels.

The proposed topology was compared with many other multilevel topologies. As a result, it shows the advantages of less TVS, reduced number of switches, and fewer DC sources. The comparison results indicate that the cascaded structures could overcome some of the disadvantages of other topologies, which reveals that the proposed topology significantly reduces the number of DC links and power switches compared to CHB, 2CLHB, and CSMLI.

Finally, the proposed structure has the lower number of DC-link sources, TSV, and THD among the mentioned topologies. Theoretical analysis were verified by simulation and experimental results in a 15-level inverter prototype.

Chapter 5

Proposed Z-source converter

5.1 Introduction

In modern electrical power systems such as distributed generation sources and industrial drives, the inverters play a fundamental role in controlling power. The limitations of the conventional inverters are the inflexibility of the current range or converted voltage. More precisely, the voltage source inverters (VSI) can only operate in the step-down voltage mode, and the current source inverters (CSI) can only operate in the step-down current mode or step-up voltage mode. In applications in which both reducing and increasing the voltage level are required, a DC-DC converter is used before the inverter.

An impedance source inverter (ZSI) was introduced in [1] for implementations of DC-DC, AC-DC, and DC-AC conversions. This inverter uses an X-shaped impedance network to connect the converter's main circuit to the power source. This structure can be applied to all power converters. The ZSI is represented as a unit-class structure that can increase or decrease the voltage in the power conversion and does not require a time delay (or dead-time) in the switches to be turned on at the same time in one leg; thus, the reliability increases. The main applications of ZSI, as described in [2-4], are distributed renewable energy power systems, hybrid electric vehicles. Their operation principles, system characteristics, modeling, and control methods are described in [5-7]. The alternative ZSI structures are presented in [8-11]. In addition to the mentioned benefits of conventional ZSIs, they have some drawbacks, such as generating a high voltage across the capacitors, generating high inrush current, and increasing the cost.

In order to deal with such problems, a structure called quasi- impedance source inverter (qZSI) was presented in [12]. This has continuous input current and low voltage stress across the capacitors. The qZSIs are applied to photovoltaic (PV) systems and motor drives [13-14]. Having a common interface between the input source and inverter side and reducing the nominal values of the used elements, are some of the major benefits of the quasi- impedance source inverters; however, the

gains are similar with impedance source inverter. In [15-16], an alternative qZSI is presented based on transformers. Thus, by choosing a high transformer's turns-ratio, higher voltage gains can be reached, though the high turns-ratio selection in transformers has some disadvantages, such as increased losses and reduced efficiency.

In [17], another structure, called L-Z-Source, is presented. It has various advantages like small inrush current, but it uses a large number of inductors to reach high voltage gains, which increases the cost, weight, and volume of the circuit. A double input Z-source structure is introduced in [18] according to the Z-source network. This structure is suitable for connecting systems with identical outputs to loads or grids. According to [19], a topology is proposed which can be applied to integrating energy sources in microgrids. This topology can control the bidirectional flow, and the topology units can be connected in series. In [20], a modular Z-source converter for the energy storage system is proposed, which can be applied in medium voltage.

In [21-23], a PWM control method is presented, which is divided into the maximum boost control and constant boost control. These methods are also aimed to increase the voltage gain. According to the method for increasing the converter gain, different circuit structures are proposed, such as switched-capacitor (SC-ZSI), switched inductor (SL-ZSI), as well as combination of them (SC/SL-ZSI) [24-25], voltage-lift circuit [26], coupled inductors [27-28] and voltage multiplier cells [29-32].

The quasi impedance-source network (qZSN) is an interesting structure that provides continuous input current and common ground between input and output. Due to its desirable features, qZSN is widely used to develop new structures. For instance, hybrid ZSIs are introduced by integrating impedance source networks and qZSN in [33], and a cascaded qZSN is developed in [34].

This chapter introduces a family of high-boost ZSIs based on switched Z-networks that can generate very high output voltage boost factors. The proposed topology produces a higher gain with the same duty cycle (D) than alternative qZSIs,

cascaded ZSIs, and SC/SL-ZSIs. Accordingly, for identical input and output voltages, it can work with lower D and higher modulation index (M), which results in lower voltage stress across the switching devices, a better output voltage quality, and a lower input current ripple. It can also mitigate the startup high inrush current.

The chapter is structured as follows. The description and analysis of the proposed switched network quasi Z-source inverter (SN-qZSI) are given in Section 5.2. Section 5.5 compares the proposed Z-source structure with several Z-source converters that have been presented in the literature. The simulation and experimental results are investigated and presented in Section 5.7. Finally, the conclusions are given in Section 5.8.

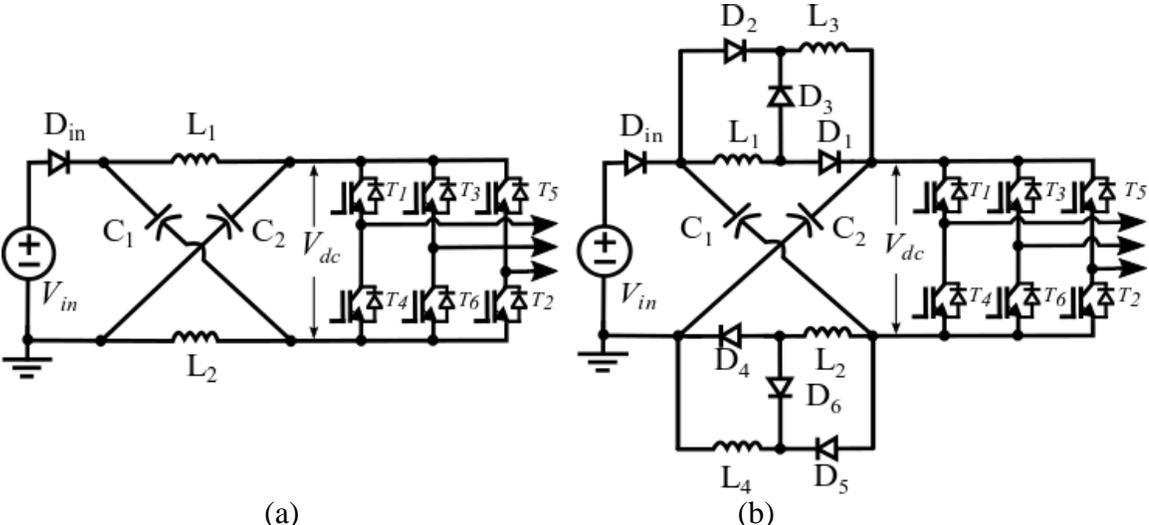


Figure 5.1 Prototype of the inverters. (a) Classical Z-source inverter [1]; (b) SL Z-source inverter [8].

5.2 Proposed switched network Z-source inverter (SN-qZSI)

Figure 5.1(a) shows the conventional ZSI inverter. This inverter’s impedance network is comprised of two separate inductors, L_1, L_2 , and two capacitors, C_1, C_2 , which are connected together in the X form. The voltage gain coefficient for the ZSI inverter is defined as follows:

$$B = \frac{V_{dc}}{V_{in}} = \frac{1}{1 - 2\frac{T_0}{T}} = \frac{1}{1 - 2D} \quad (5.1)$$

where T_0 is the state time of shoot through, T is the switching period, and D is the duty cycle of shoot through.

Fig. 5.1(b) shows another structure, the SL-ZSI inverter. This inverter is comprised of four inductors (L_1, L_2, L_3 and L_4), two capacitors (C_1 and C_2), and seven diodes ($D_1, D_2, D_3, D_4, D_5, D_6$ and D_{in}). L_1, L_3, D_1, D_2, D_3 and L_2, L_4, D_4, D_5, D_6 combinations are the upper and lower SL cells, respectively. With these two cells and a proper switching pattern, the energy can be stored and transferred to the output efficiently. The voltage gain coefficient for the SL-ZSI inverter is higher:

$$B = \frac{V_{dc}}{V_{in}} = \frac{1 + \frac{T_0}{T}}{1 - 3\frac{T_0}{T}} = \frac{1 + D}{1 - 3D} \quad (6.2)$$

In this chapter, the concept of SL technique and Z impedance switching are used for the proposed high performance Switched Network ZSI (SN-ZSI) structure. The proposed SN-ZSI can produce a very high output voltage gain (B). In addition, the proposed structure has a higher amplification coefficient ($G=M.B$, where M is defined as modulation index) compared to the other structures in a stable working cycle. The new structure is illustrated in Figure 5.2. In the following subsection, the structure analysis details are surveyed, discussed, and confirmed through the simulation results.

Figure 5.2 shows the proposed SN-ZSI circuit, which consists of four capacitors (C_1, C_2, C_3, C_4), four inductors (L_1, L_2, L_3, L_4), and five diodes (D_1, D_2, D_3, D_4, D_5). The combination of L_1, C_1 , and L_2, C_2 forms the upper network impedance, and the combination of L_4, C_4 , and L_3, C_3 forms the lower network impedance. The main features of the suggested SN-qZSI structure are the following:

- Only two capacitors are added to the circuit, and the two diodes less than the number of diodes in the SL-qZSI structure have been used.
- There is a common interface between the input DC voltage and the inverter, which mitigates the high inrush current at the turn-on of the inverter.
- The voltage stress of the elements is decreased. Therefore, the cost decreases, and reliability increases.
- The duty cycle range ($D_{min} < D < D_{max}$) is reduced. Thus, a higher modulation index (M) can be used, leading to a higher output voltage quality of the inverter.

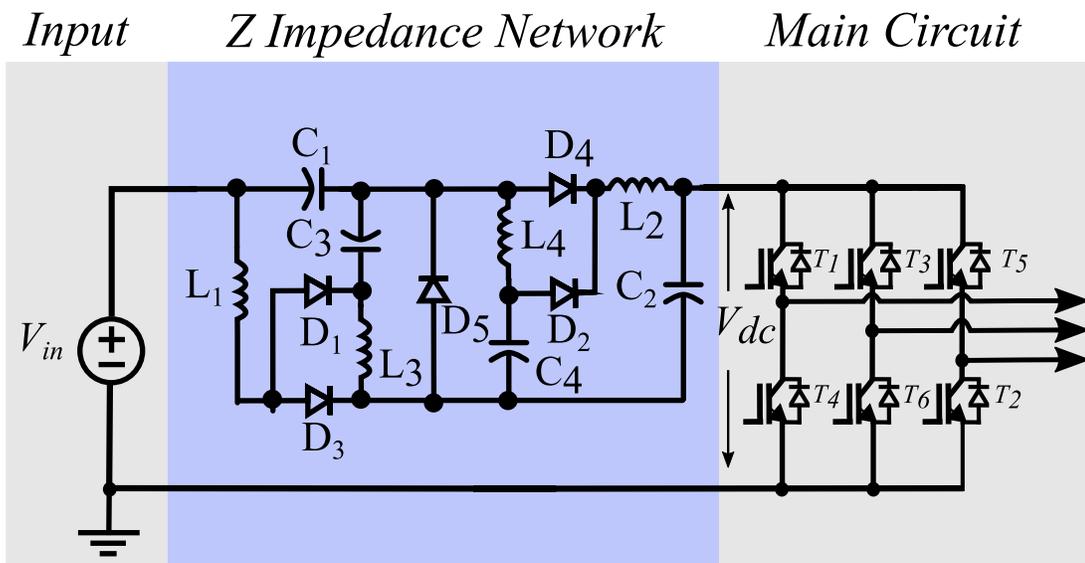


Figure 5.2: Proposed SN-ZSI.

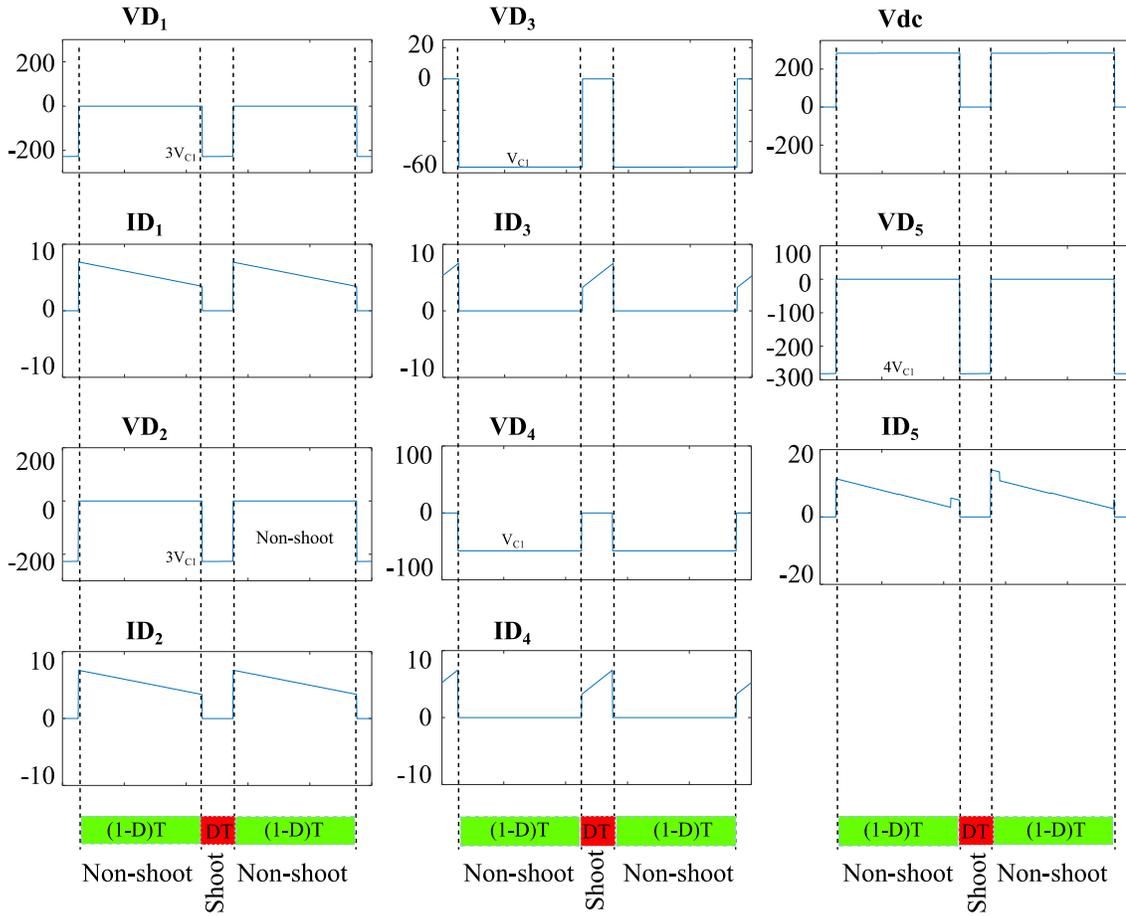


Figure 5.3 The diodes in Shoot and Non-shoot through states

5.3 Steady-State Operation Principles of SN-ZSI

The suggested inverter operation is similar to the SL-ZSI converter. Therefore, the different states of the suggested inverter are divided and discussed into two parts: the Shoot through State (STS) and Non-shoot through State (NTS). Assuming that the capacitors are large and equal, their voltages are:

$$V_{C1} = V_{C2} \quad (5.3)$$

$$V_{C3} = V_{C4} \quad (5.4)$$

Figure 5.3 shows the voltage and current of diodes in both states. In the STS, D_3, D_4 are on, whereas the diodes D_1, D_2, D_5 are off. Figure 5.4(a) shows the SN-ZSI

circuit in the STS. In this circuit, the L_3C_3 the branch is paralleled with the L_4C_4 branch

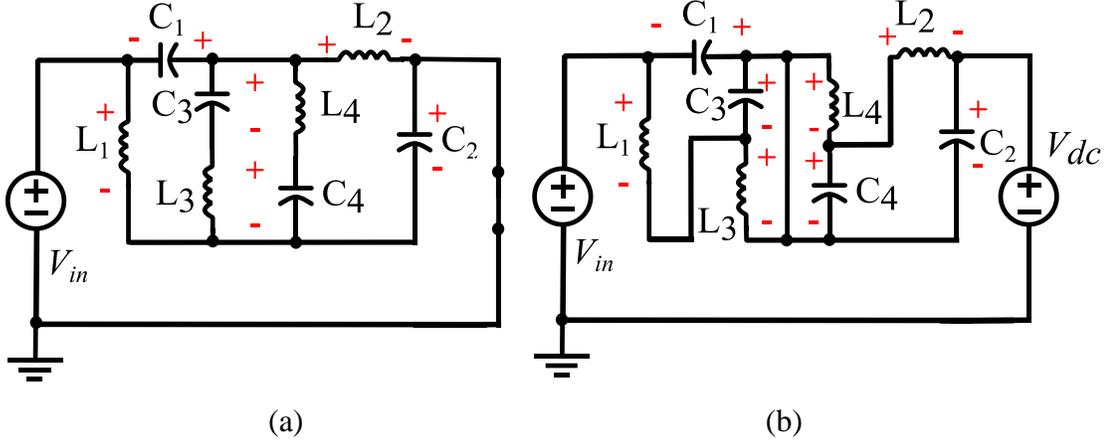


Figure 5.4: Equivalent circuits. (a) Shoot through state. (b) Non-shoot through state.

and the input voltage is equal to $V_{C1} + V_{L2}$ or $V_{C2} + V_{L1}$. In this way, the following expressions can be written:

$$L_1 \frac{di_{L1}}{dt} = V_{L1-on} = V_{in} + V_{C2} \quad (5.5)$$

$$L_2 \frac{di_{L2}}{dt} = V_{L2-on} = V_{in} + V_{C1}, \quad (5.6)$$

$$L_3 \frac{di_{L3}}{dt} = V_{L3-on} = V_{in} + V_{C1} + V_{C2} - V_{C3}, \quad (5.7)$$

$$L_4 \frac{di_{L4}}{dt} = V_{L4-on} = V_{in} + V_{C1} + V_{C2} - V_{C4}. \quad (5.8)$$

Based on the voltage-second law [20], inductors in one period have an average voltage of zero, so:

$$DV_{L-on} + (1 - D)V_{L-off} = 0, \quad (5.9)$$

where V_{L-ON} and V_{L-OFF} are the voltage of the inductor during the STS and NTS, respectively.

In the NTS, D_1, D_2, D_5 are on, whereas the diodes D_3, D_4 are off. Figure 5.4(b) shows the SN-ZSI circuit in the NTS. Therefore, the voltage of inductors during the NTS can be calculated as:

$$L_1 \frac{di_{L1}}{dt} = V_{L1-OFF} = V_{C3} - V_{C1}, \quad (5.10)$$

$$L_2 \frac{di_{L2}}{dt} = V_{L2-OFF} = V_{C4} - V_{C2}, \quad (5.11)$$

$$L_3 \frac{di_{L3}}{dt} = V_{L3-OFF} = -V_{C3}, \quad (5.12)$$

$$L_4 \frac{di_{L4}}{dt} = V_{L4-OFF} = -V_{C4}. \quad (5.13)$$

The currents i_{L1} and i_{L3} are linear. They increase during the STS and decrease during the NTS. The voltage of L_1 is equal to $(V_{in} + V_{C2})$ and $(V_{C3} - V_{C1})$ in the STS and NTS respectively. In addition, the voltage of L_3 is equal to $(V_{in} + V_{C1} + V_{C2} - V_{C3})$ and $(-V_{C3})$ in the two states as well. It is clear that in the STS, the voltages of L_1 and L_3 are positive, whereas in the NTS are negative. By using (5.5), (5.8) and (5.9), V_{C3} can be obtained as:

$$V_{C3} = V_{C4} = D(V_{C1} + V_{C2} - V_{in}). \quad (5.14)$$

In the main circuit of Figure 6.4(b), we have:

$$V_{DC} = V_{in} + V_{C1} + V_{C2}. \quad (5.15)$$

Then, by using (6.5), (6.6), (6.9), (6.11), (6.12), and (6.13), the DC-link peak voltage \hat{V}_{dc} can be obtained:

$$\hat{V}_{dc} = \frac{2V_{in}}{19D^2 - 12.5D + 2} = BV_{in}, \quad (5.16)$$

where

$$B = \frac{2}{19D^2 - 12.5D + 2} \quad (5.17)$$

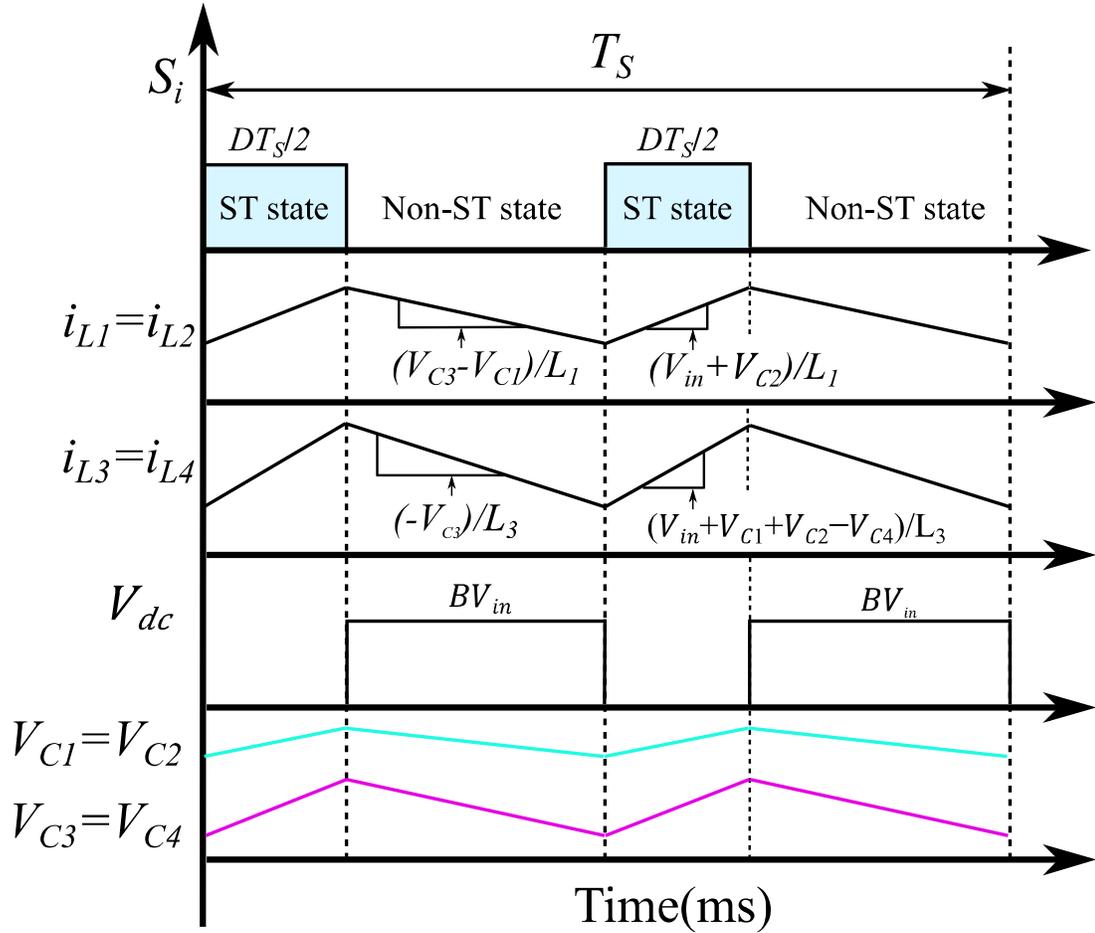


Figure 5.5 Waveforms of the proposed converter in the DC side.

is the boost factor of the proposed topology. The maximum ac output phase voltage of the SN-ZSI can be expressed as:

$$\frac{\hat{V}_{ac}}{\hat{V}_{dc}/2} = M \quad (5.18)$$

where M is the modulation index. Using (5.16) and (5.18), we have:

$$\hat{V}_{ac} = M \cdot B \cdot \frac{V_{in}}{2} = G \cdot \frac{V_{in}}{2}, \quad (5.19)$$

where

$$G = M \cdot B \quad (5.20)$$

is the buck-boost factor. It can be changed from zero to infinite ($0 \rightarrow \infty$) by controlling the value of D and M . The duty cycle of shoot through (D) is bounded by the modulation index (M), which has the following maximum threshold:

$$M \leq 1 - D \quad (5.21)$$

The boost factor in (5.17) shows that if D changes between 0 to 0.274, B varies from one to infinite. However, the infinite value of B cannot be achievable because of the parasitic effects of physical components. Moreover, if the D value is set to a high value in order to generate a high boost gain, the modulation (M) needs to be so small, as mentioned in (5.19), that it will produce high harmonic distortion (THD). In summary, small M is not implemented since it has a negative effect on output waveform quality and increases output power losses due to its higher-order harmonics. In comparison with conventional ZSI, the proposed topology produces a higher voltage gain with the same M . Therefore, in the equal voltage conversion ratio (boost factor, B), the proposed ZSI converter needs a larger modulation index M to increase the output voltage's quality. According to (5.17) and (5.18), with a very small D , a considerable amount of M is achievable, which is advantageous.

5.4 Parameter Design of the Network Impedance

For selecting an appropriate inductor and capacitor, it is essential to calculate the inductor current and capacitor ripples. Figure 6.5 shows the DC side theoretical waveforms of the proposed converter. According to this figure and Figure 6.4(a), in the STS, the inductors will be charged by capacitors, therefore:

$$V_{L1} = V_{L2} = V_{C1} = V_{C2} = L_1 \frac{di_{L1}}{dt} \quad (5.22)$$

$$V_{L3} = V_{L4} = V_{C3} = V_{C4} = L_3 \frac{di_{L3}}{dt}, \quad (5.23)$$

because the circuit is symmetric, and the capacitances and inductances are the same. Following relations can be obtained:

$$\begin{cases} V_{C3} = V_{C4} = D(V_{C1} + V_{C2} - V_{in}) \\ V_{dc} = V_{in} + V_{C1} + V_{C2} \end{cases} \quad (5.24)$$

so from (5.22), (5.23), and (5.24), the value of inductors can be extracted by:

$$L_1 = \frac{4V_{in}D(1-D)^2}{f_s \Delta i_{L1} K_{nsh} (6D^2 - 12D + 3)} \quad (5.25)$$

$$L_3 = \frac{4V_{in}D(1-D)}{f_s \Delta i_{L2} K_{nsh} (6D^2 - 12D + 3)}, \quad (5.26)$$

where K_{nsh} is the number of STS in one switching period, (normally 1), and $\Delta i_{L1}, \Delta i_{L2}$ are the current ripples of L_1 and L_2 , respectively.

For capacitors, we have:

$$\begin{cases} i_{C1} = C_1 \frac{dV_{C1}}{dt} \\ i_{C3} = C_3 \frac{dV_{C3}}{dt} \end{cases} \quad (5.27)$$

In the STS, the current through C_3, C_4 capacitors are equal to the L_3, L_4 , inductors' current; hence, from Figure 5.4(a), Figure 5.5 and (5.27) the capacitors can be calculated as

$$C_1 = \frac{D(i_{in(AV)} - i_{L1(AV)})}{f_s \Delta i_{C3} K_{nsh}} \quad (5.28)$$

$$C_3 = \frac{D i_{L3(AV)}}{f_s \Delta i_{C4} K_{nsh}} \quad (5.29)$$

where $i_{L1(AV)}, i_{L3(AV)}, i_{in(AV)}$ are the average current of L_1, L_3, V_{in} , and $\Delta i_{C3}, \Delta i_{C4}$ are the current ripples of C_3 and C_4 respectively.

5.5 Comparison Study of High Boost Impedance Sources Inverters

The proposed structure's performance is compared with the conventional non-isolated high-boost qZSIs. An analysis of the comparison includes the output voltage gain, the number of active and passive components that are used at the impedance network, and the voltage and current stress.

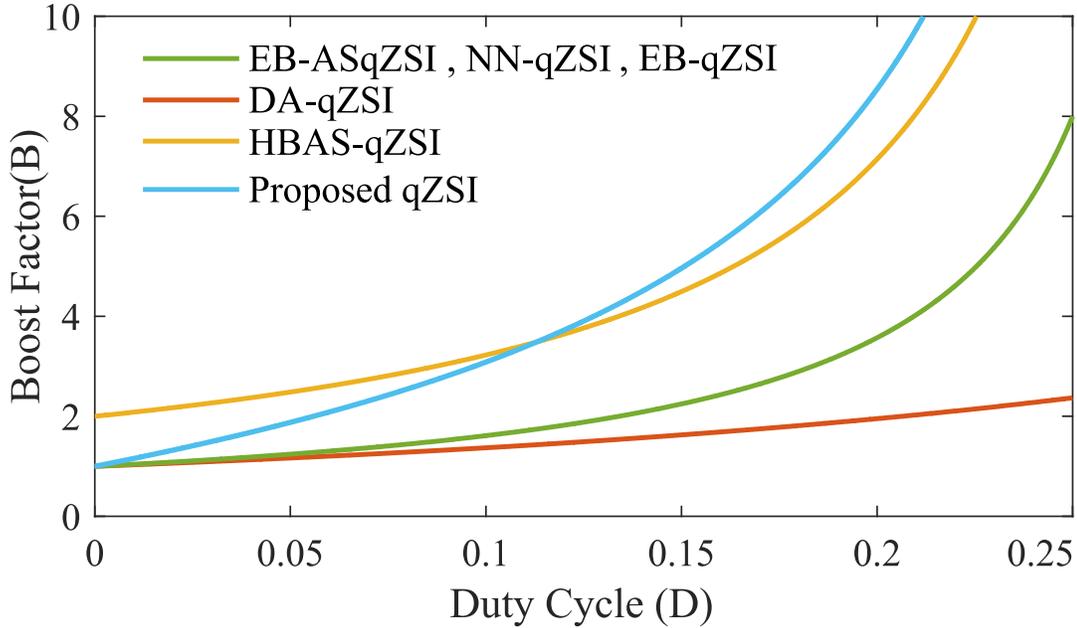


Figure 5.6 Boost factor versus shoot through duty cycle

5.5.1 Output voltage gain (boost ability)

Figure 5.6 shows a comparative study of boost factor, B , versus shoot through duty cycle, D , of the proposed inverter with the existing inverters. The details of each inverter are in Table 5.1. As can be seen, the boost factor (B) of the SN-qZSI is higher than EB-qZSI [3], DA-qZSI [9], HBAS-qZSI [25], EB-ASqZSI [26], NN-qZSI [27] for the same input voltage and shoot through duty cycle. According to [19], if the constant boost control is applied to the proposed topology, the shoot through duty cycle D is bounded by the modulation index M , so $D = 1 - \sqrt{3}M/2$. Therefore, the corresponding buck-boost factor G is as follows:

$$G = M.B = \frac{1.4M}{10M^2 - 9M + 6}. \quad (5.30)$$

In Figure 5.7, the buck-boost factor, G , against the modulation index, M , is plotted for mentioned six topologies. Figure 5.7 illustrates that with the proposed

Table 5.1 Comparison of the proposed qZSI with other topologies.

	EB-qZSI [3]	DA-qZSI [9]	HBAS-qZSI [25]	EB-ASqZSI [26]	NN-qZSI[27]	Proposed qZSI
<i>Boost Factor (B)</i>	$\frac{1}{1 - 4D + 2D^2}$	$\frac{1}{(1 - D)(1 - D)^2}$	$\frac{2}{1 - 4D + 2D^2}$	$\frac{1}{1 - 4D + 2D^2}$	$\frac{1}{1 - 4D + 2D^2}$	$\frac{2}{2 - 12.5D + 19D^2}$
<i>Inductor</i>	4	4	2	2	4	4
<i>Capacitor</i>	4	4	3	2	4	4
<i>Diode/Switch</i>	5/0	5/•	5/1	4/1	5/•	5/0
<i>Capacitor Voltage Stresses (V_C/V_{DC})</i>	$(1 - D)^2B, D(1 - D)B, D(2 - D)B, (1 - 3D + 2D^2)B$	DB, (1-2DB),(1-D)(1-2D)B	B/2, (1-2D)B/2	B, (1-2D)B	D(2-D)B, D(3-D)	$(1 - D)^2B, (1 - D)B$
<i>Diode Voltage Stresses (V_D/V_{DC})</i>	B, DB, (1-D)B	B, 2DB, (1-2D)B, D(3-2D)B, (1-D)(1-2D)B	B/2, DB, (1-D)B	B, 2DB, (1-2D)B	B, DB, (1-D)B	B, DB, (1-D)B
<i>Voltage Stress of switch S_7 (V_{S7}/V_{DC})</i>	-	-	B/2	B	-	-
<i>Inductor Current Stresses (I_L/I_{PN})</i>	$(1 - D)B, (1 - D)^2B$	$(1 - D)B, (1 - D)^2B$	$(1 - D)B, (1 - D)^2B$	$(1 - D)B, (1 - D)^2B$	$(1 - D)B, (1 - D)^2B$	$(1 - D)B, (1 - D)^2B$
<i>Shoot through Current Stresses (I_{sh}/I_{PN})</i>	$2[1 - D + (1 - D)^2]B$	$[2 - D + 2(1 - D)^2](1 - D)B$	$(1 - D)B + (1 - D)^2B$	$(1 - D)B + (1 - D)^2B$	$2[1 - D + (1 - D)^2]B$	$2[1 - D + (1 - D)^2]B$
<i>Average DC-link Current (I_{PN})</i>	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$	$\frac{(1 - D)\hat{V}_{ac}}{R_i}$
<i>Buck-Boost Factor ($G=MB$)</i>	$\frac{2M}{3M^2 - 2}$	$\frac{4}{3\sqrt{3}M^2 - 3M}$	$\frac{4M}{3M^2 - 2}$	$\frac{2M}{3M^2 - 2}$	$\frac{2M}{3M^2 - 2}$	$\frac{1.4M}{10M^2 - 9M + 6}$

qZSI, the inverter bridge can be modulated with a higher modulation index, M , to achieve the same buck-boost factor. As a result, proposed inverter able to generate output voltage waveforms with higher quality and lower total harmonic distortion (THD). An enhanced output waveform is the result of a high modulation index.

5.5.2 Number of Components

Table 5.1 also compares the number of components used at the impedance network for high-boost qZSIs. The table indicates that the proposed topology can be implemented using the same passive and active components as the EB-qZSI, DA-qZSI, and NN-qZSI. To have high gain, the HBAS-qZSI and EB-ASqZSI references use one extra switch, which increases the cost of the topology. It means that these topologies need one additional driver and a more complex controller. Therefore, it can be concluded that EB-qZSI, DA-qZSI, NN-qZSI references, and the proposed topology have a lower installation cost.

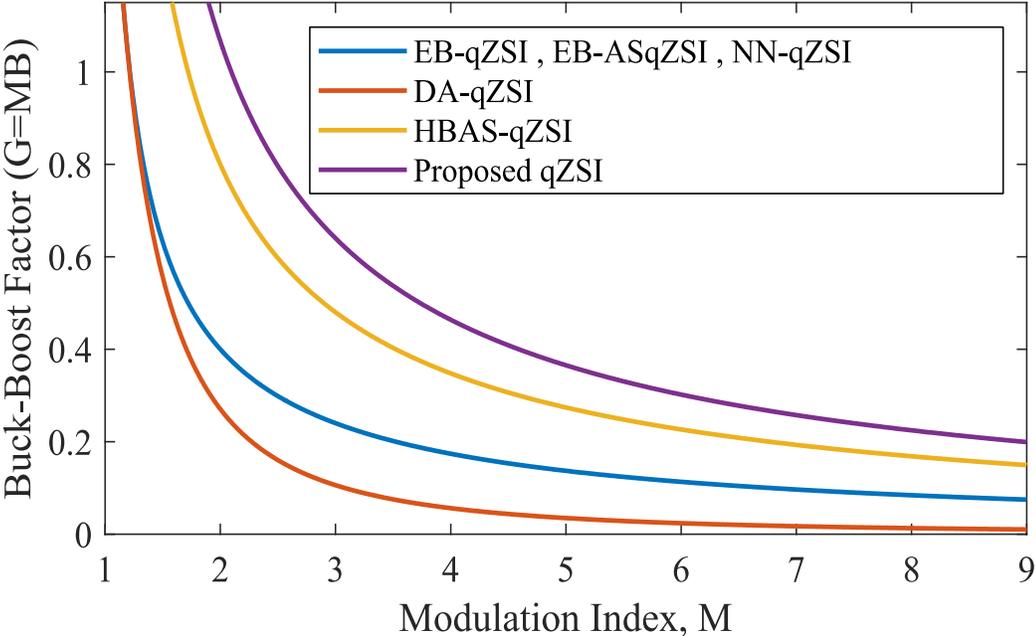


Figure 5.7 Ratio of the Buck-boost factor G and the modulation index M.

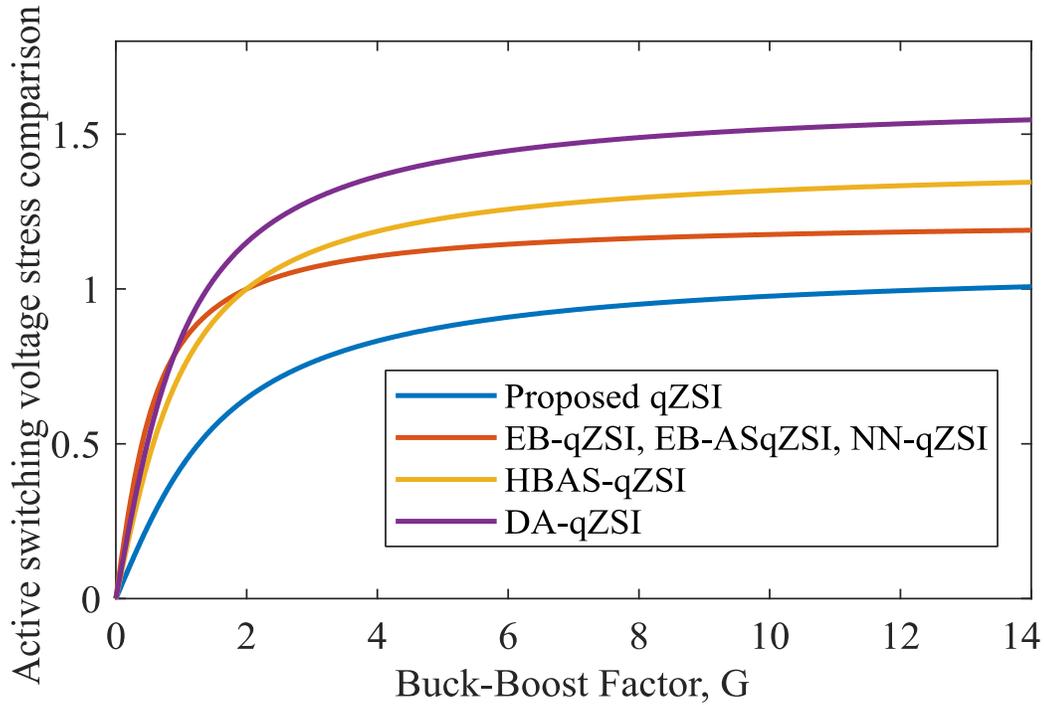


Figure 5.8 Comparison of voltage stress on active switching devices

5.5.3 Voltage and Current Stresses

Due to varying methods of control, input voltages, and load conditions, impedance network-type power inverters would undergo varied current and voltage stresses. To compare these six qZSI topologies precisely, the AC side circuit is represented by an equivalent DC load ($Z_l=R_l+sL_l$) and a single active switch [7]. For the corresponding voltage stresses on the passive elements and switching devices of the topologies of Table 5.1, we assume the same modulation index, DC input voltage, and output power. An active switching device's voltage stress is described as the peak DC-link voltage ratio to an equivalent DC voltage GV_{DC} , as demonstrated [17]. In the same DC input voltage condition, the voltage ratio deals with the cost of achieving the same voltage boost. The corresponding voltage stress ratio of a single active switch of the equivalent DC load can be derived as:

$$\frac{\hat{V}_{PN}}{GV_{DC}} = \frac{BV_{DC}}{GV_{DC}} = \frac{4}{3} \left[\sqrt{\frac{2}{3} + \left(\frac{8}{9G}\right)^2} - \left(\frac{8}{9G}\right) \right]. \quad (5.31)$$

The voltage stress across the semiconductor switches of the proposed inverter and other inverter topologies is illustrated in Figure 5.8. This figure depicts that the suggested inverter implies less voltage stress on switches than other topologies in the same given voltage gain G .

The capacitor voltage stress comparison is presented in Figure 5.9. The capacitor voltage stress is calculated by dividing the capacitor voltage by the equivalent DC voltage GV_{DC} [19]. For most of the buck-boost factor G values, the voltage stress of C_3 and C_4 in the proposed converter has lower capacitor voltage stress than in EB-qZSI, HBAS-qZSI, EB-ASqZSI, NN-qZSI, except for the C_4 in the DA-qZSI. The voltage stresses of C_1 and C_2 are constant, and do not depend on the gain of the proposed inverter; actually, they depend on the input voltage.

The inductor current stress comparison between the proposed inverter and the other inverter topologies is presented in Figure 5.10. It can be observed that for obtaining the same buck-boost factor G , the inductor current stress of L_1 ($=L_2$) of the proposed method is the same as the EB-qZSI(L_1, L_2), HBAS-qZSI (L_1), EB-ASqZSI (L_2), NN-qZSI(L_1, L_4) and the DA-qZSI (L_4). The inductor current stress of L_3 ($=L_4$) of the proposed inverter is the same as the EB-qZSI(L_3, L_4), EB-ASqZSI (L_1), and NN-qZSI(L_2, L_3), but lower than the HBAS-qZSI (L_2), and higher than DA-qZSI (L_1, L_2, L_3). This is because the proposed topology can produce a higher buck-boost factor by using a small shoot through duty ratio.

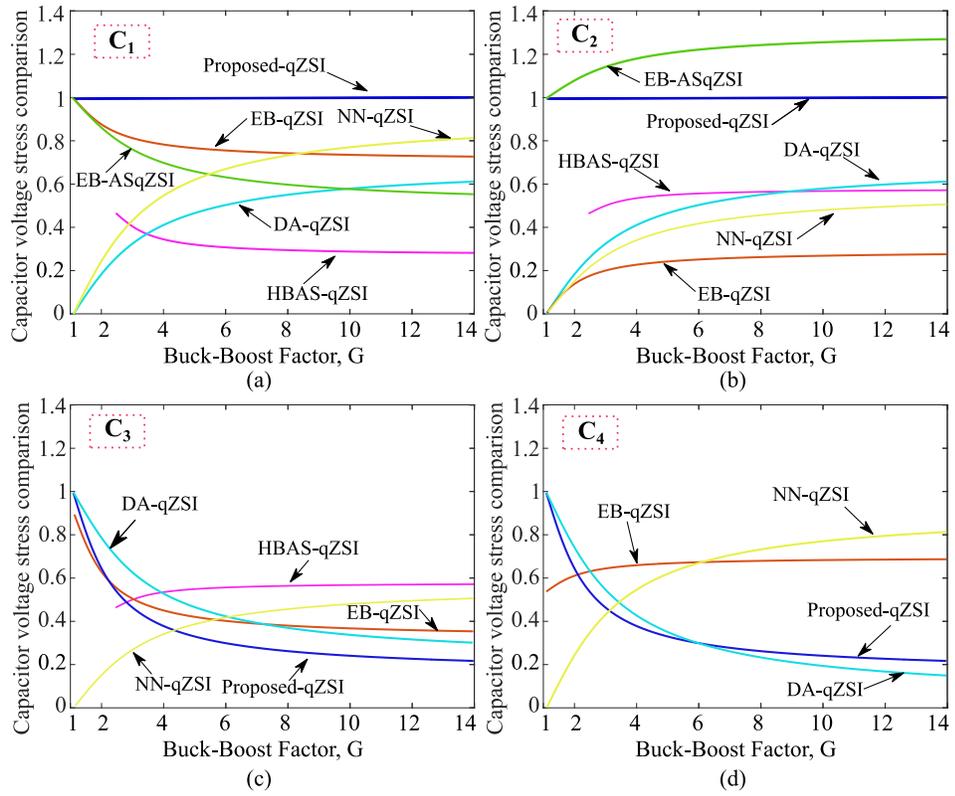


Figure 5.9 Comparison of capacitor voltage stresses. (a) Voltage stress on C_1 , (b) Voltage stress on C_2 , (c) Voltage stress on C_3 , (d) Voltage stress on C_4 .

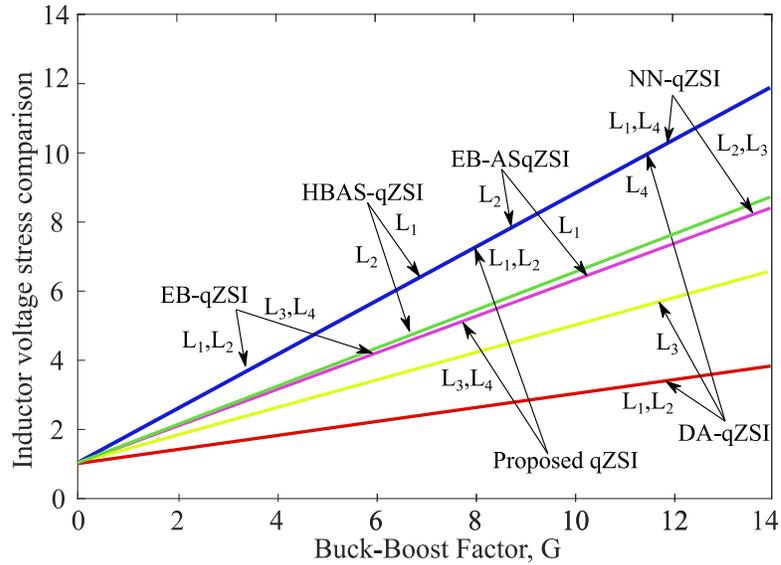


Figure 5.10 Comparison of inductor current stresses.

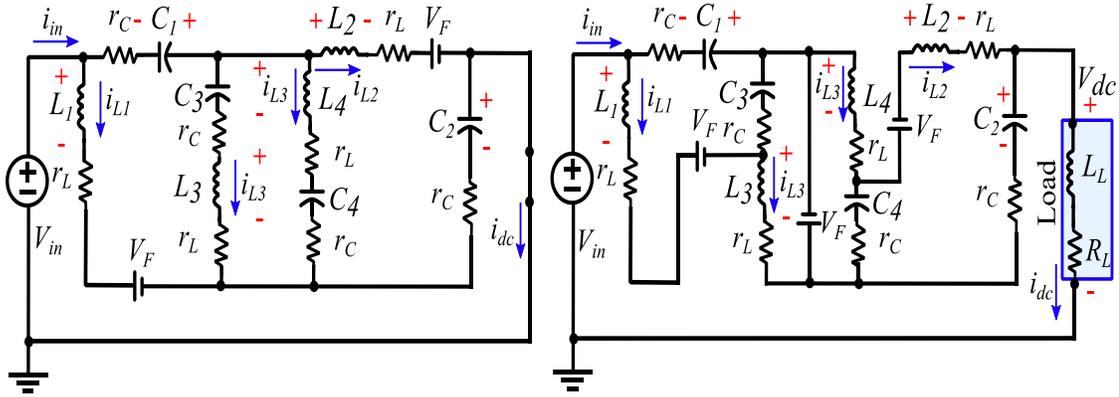


Figure 5.11 Equivalent circuits in (a) Shoot through state, (b) Non-shoot through state.

5.6 Comparison of Power Loss and Efficiency

Due to evaluating the power losses of impedance network-based inverter structures, the diodes are considered as ideal diodes in series with its forward voltage drop V_F and intrinsic resistances r_D . The MOSFETs are represented by ideal lossless semiconductor switches in series with the equivalent drain-to-source resistance r_{DS} . Inductors and capacitors are considered by ideal passive components with their equivalent series resistances, r_L , and r_C , respectively. In addition, the forward conduction losses are the same model for all of the diodes (Figure 5.11).

Some assumptions are made in order to simplify the power losses computation for the suggested inverter: 1) Voltage and current ripples in capacitors and inductors are ignored, 2) The diode's turn-on loss is so minimal that it may be overlooked, 3) Switch and diode off-state blocking losses are ignored, 4) Capacitor ripple loss is minimal enough to be neglected.

5.6.1 Inductor Losses

The inductor's losses are divided into winding copper and core losses. The winding copper losses are determined mainly by the resistance of the copper winding and the RMS current of the inductor. According to Micro-metal's datasheet, core losses per unit volume can be determined (Core model: SK300125A). However, due

to the slight inductor current ripples, the core losses are negligible in comparison to the overall copper conduction losses. Inductor's total conduction loss can be calculated as follows:

$$P_{I\ Loss} = 2D^2r_L(i_{L1_{RMS}}^2 + i_{L3_{RMS}}^2) + 2(1-D)^2r_L(i_{L1_{RMS}}^2 + i_{L2_{RMS}}^2 + i_{L3_{RMS}}^2 + i_{L4_{RMS}}^2) \quad (5.32)$$

where r_L is the inductor's equivalent series resistance (ESR) as given in Table 5.2.

5.6.2 Capacitor Losses

In Table 5.2, the equivalent series resistance (ESR) of capacitors is used to calculate the total conduction loss of the capacitor as follows:

$$P_{C\ Loss} = D^2r_C \left[i_{L2_{RMS}}^2 + 2i_{L3_{RMS}}^2 + 2i_{L4_{RMS}}^2 + (i_{L2_{RMS}} - i_{dc_{RMS}})^2 \right] + (1-D)^2r_C \left[(i_{in_{RMS}} - i_{L1_{RMS}})^2 + (i_{in_{RMS}} - i_{L3_{RMS}})^2 + i_{L4_{RMS}}^2 + (i_{L2_{RMS}} - i_{dc_{RMS}})^2 \right]. \quad (5.33)$$

where r_C is the capacitors's equivalent series resistance (ESR).

5.6.3 MOSFET Losses

There are two types of power losses in active switches: switching losses that occur during the ON and OFF periods of the switching state and conduction losses. Calculating the total switching losses of MOSFETs can be done as follows:

$$P_{Sw\ Loss} = (t_{on} + t_{off})f_{sw}V_{out}(2-D)i_{in_{RMS}}/2 \quad (5.34)$$

where, f_{sw} is the switching frequency, V_{out} is the inverter's output voltage, i_{in} is the average current of DC power supply, and t_{on} , t_{off} are the turn-on and turn-off times of MOSFETs, respectively.

The total conduction loss of switches is calculated as:

$$P_{Con Loss} = r_{DS} \left[\frac{2}{3} D(2-D)^2 i_{in_{RMS}}^2 + \frac{1.08(1-D)^3 P_{out}^2}{V_{in}^2 M^2 B^2 \cos^2(\varphi)} \right], \quad (5.35)$$

in this formula, r_{DS} is the resistance between drain and source of the MOSFET, P_{out} is the output power, and $\cos(\varphi)$ is power factor of the load.

5.6.4 Diode Losses

There are two types of power losses on the diode: conduction losses in the forward voltage drop, V_F , and losses in the forward resistance, r_F . When the ripples of the inductor current and r_F are small enough, then the overall conduction losses of diodes can be calculated as follows:

$$P_{D Loss} = 3V_F(1-D)i_{in} \quad (5.36)$$

where V_F is the forward voltage drop of each diode for the loss-related parameters detailed in Table 5.2. Figure 5.12 shows the power losses for each component of the proposed SN-ZSI.

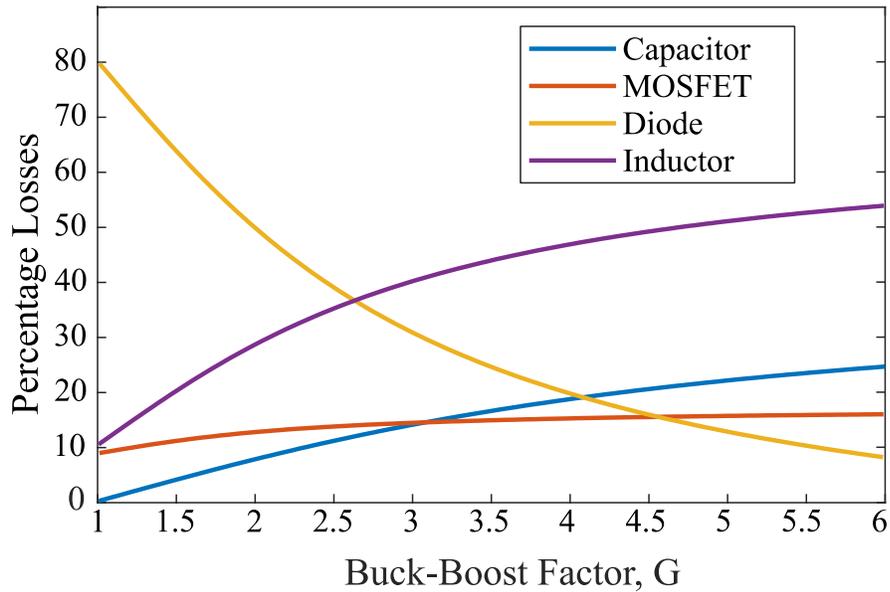


Figure 5.12 Based on the proposed topology, percentage of losses versus buck-boost factor.

Table 5.2. Power Loss Calculation Parameters

Components	Type
Parasitic resistance of inductors (r_L)	120m Ω
ESR of capacitors (r_C)	100m Ω
Diode (RURG3060CC)	$V_F(\max)=1.3V$
MOSFET S1~S6 (FCH040N65S3)	$r_{DS}=35.4m\Omega$
Inductor core	SK300125A

5.6.5 Efficiency

The efficiency is:

$$\eta_{eff} = \frac{V_{dc}I_{dc}}{P_{Total-Loss} + V_{dc}I_{dc}} \quad (5.37)$$

where

$$P_{Total-Loss} = P_{I Loss} + P_{C Loss} + P_{Sw Loss} + P_{Con Loss} + P_{D Loss} \quad (5.38)$$

by using (5.32), (5.33), (5.34), (5.35), and (5.36), the efficiency can be calculated:

$$\eta_{eff} = \frac{1}{A + B + C + 1} \quad (5.39)$$

where

$$\begin{cases} A = \frac{4r_L (1 - D)^3 [1 - (1 - D)^2]}{3R_L (6D^2 - 12D + 3)^2} [(1 - D)^2 + D^2] \\ B = \frac{8r_C D^2 (1 - D)^3 [1 - (1 - D)^2]}{R_L (6D^2 - 12D + 3)^2} \\ C = \frac{9V_F}{4V_{in}} (1 - D). \end{cases} \quad (5.40)$$

where R_L is the load resistance. In Figure 5.13, the calculated efficiency of the proposed topology and the other high-boost inverters is compared to the buck-boost factor based on the parasitic parameters in Table 5.2. According to this figure, the

proposed converter has a higher efficiency than the other mentioned topologies except for DA-qZSI.

Table 5.3 Parameters used for Simulation and Experiments.

Parameters/Components	Values
Input voltage, V_{in}	80V
Inductors ($L1 = L2 = L3 = L4$)	0.5mH
Capacitors ($C1 = C2 = C3 = C4$)	500uF
Switching frequency, f_s	30KHz
Fundamental frequency, f	50Hz
Modulation index, M	0.85
Duty cycle	0.15
Power MOSFETs	FCH040N65S3/600V, 30A
Load	40 Ω +10mH

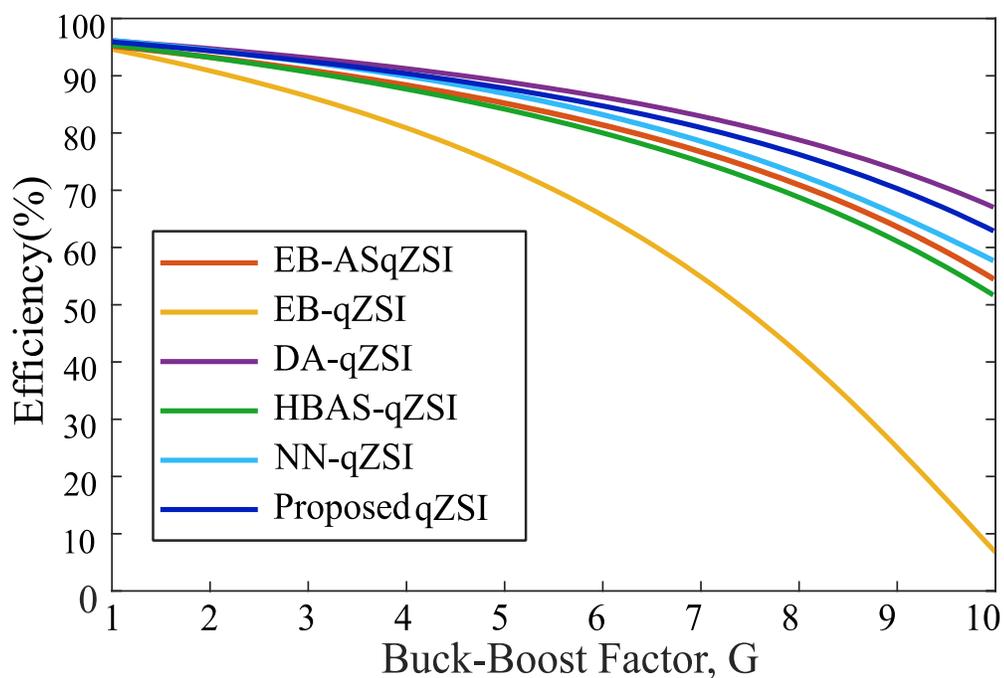


Figure 5.13: Efficiency comparison.

5.7 Simulation and Experimental Results

Simulated validation studies for this converter are conducted using MATLAB/Simulink. The introduced structure, shown in Figure 5.2, has been simulated. The values of circuit parameters are shown in Table 5.3. As part of the proposed topology, Figure 5.14 illustrates the control block diagram for generating the control signals. About the application, as we move forward with our energy efficiency efforts, converters offer a potential solution to the growing demand for energy and the increasing environmental impact of conventional power systems. Increasingly, power electronic converters are being employed for active power filtering and compensation [35]. Figure 5.15 shows the simulation results. In the simulation, the shoot through state (STS) duty cycle, D , and modulation index, M , are 0.15 and 0.85, respectively.

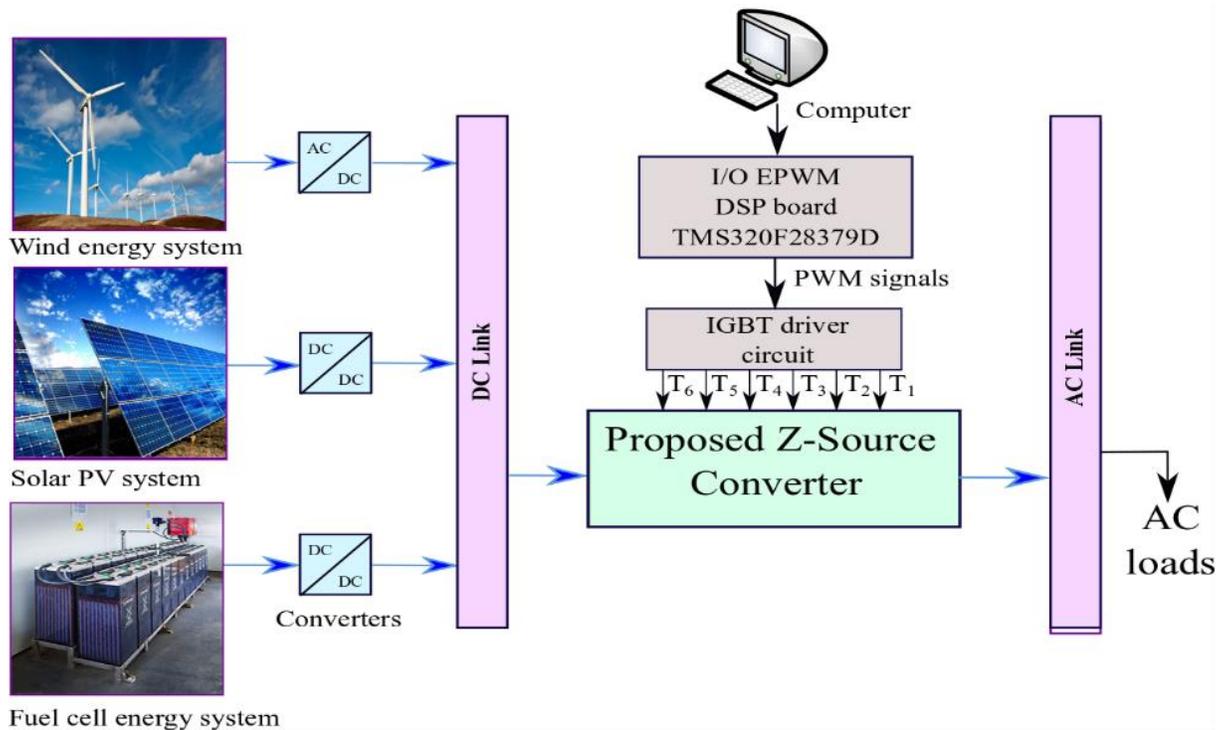


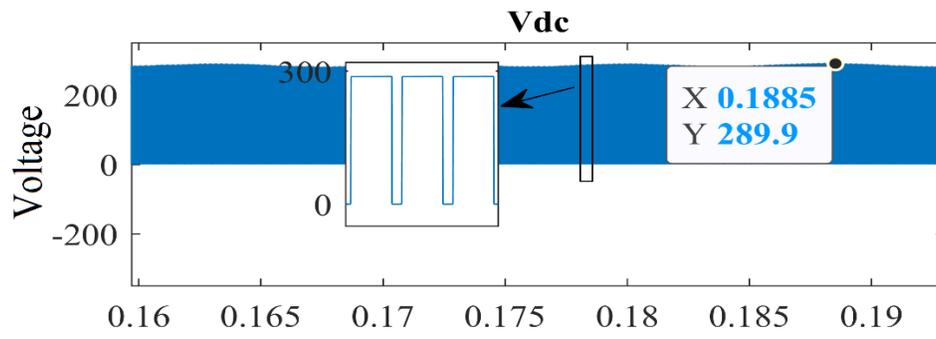
Figure 5.14 The experimental system's block diagram.

Figure 5.15(a) shows the V_{DC} after the Z network, close to 289.9V. In Figure 5.15(b) and Figure 5.15(c), the peak value of V_{AB} (Line to line) and V_{ph} (Load) are 289.3V and

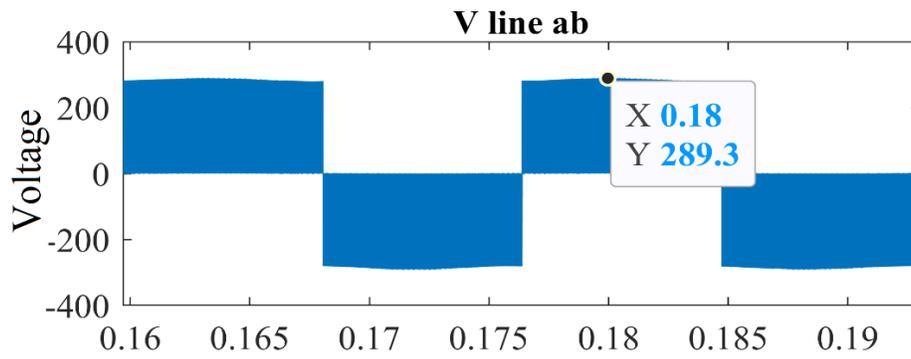
192.4V, respectively. The current in the load can be seen in Figure 5.15(d), in which the maximum current is 2.43A.

Figure 5.15(f) shows the inrush current of SN-qZSI, which is close to 55A. The values of inrush currents in EB-qZSI, DA-qZSI, HBAS-qZSI, EB-ASqZSI, and NN-qZSI topologies are provided in Table 5.4. These values were obtained by simulating different topologies using the same components and input/output characteristics. According to Table 5.4, the proposed structure has lower inrush current than EB-qZSI, DA-qZSI, NN-qZSI except for EB-ASqZSI, HBAS-qZSI. However, EB-ASqZSI and HBAS-qZSI, during the steady-state, the Maximum input currents reach values higher than 50A, much higher than our proposal (15A). This impacts on the stress on the switches and the input source (battery).

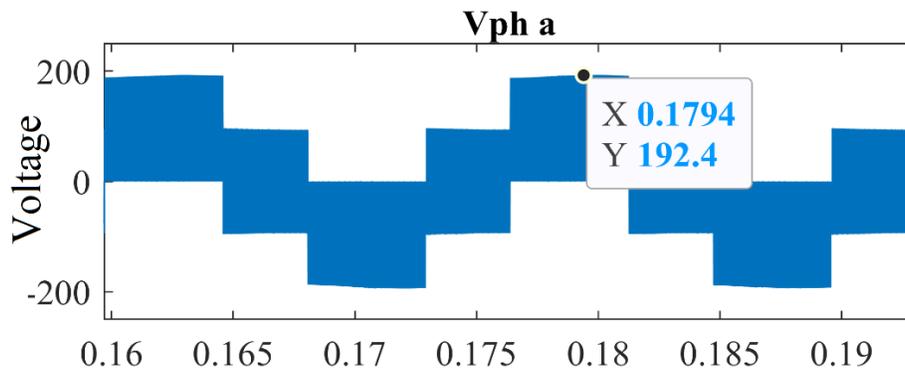
Therefore, in some topologies, a soft-start is mandatory by adjusting the duty cycles of the switches during the turn-on, but in others the currents are too high even during whole steady state. In our proposal, the inrush current is moderate, so even without soft-start it has reasonable values, and can be improved further using soft-start.



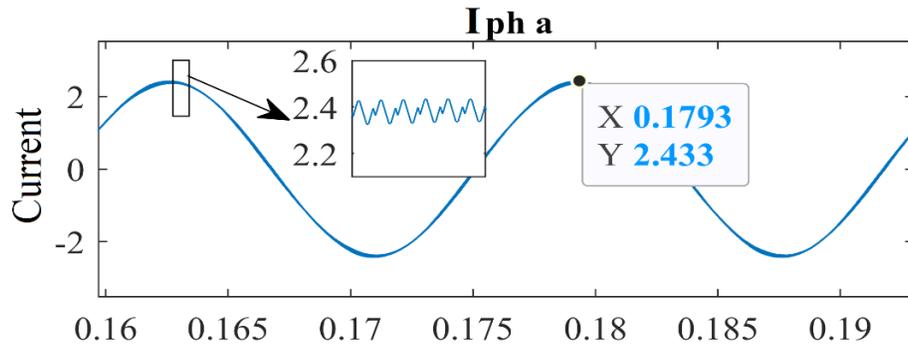
(a)



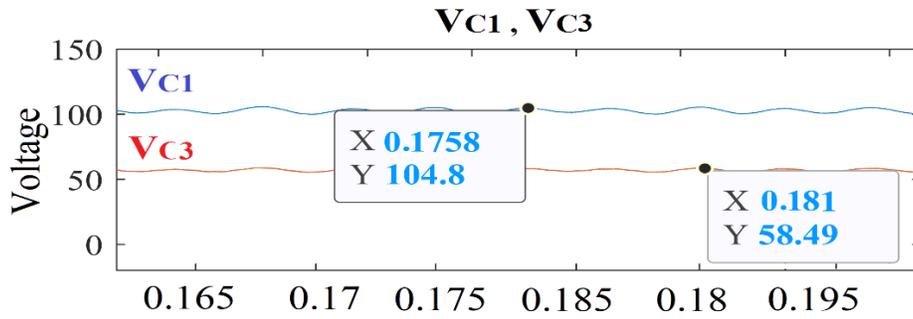
(b)



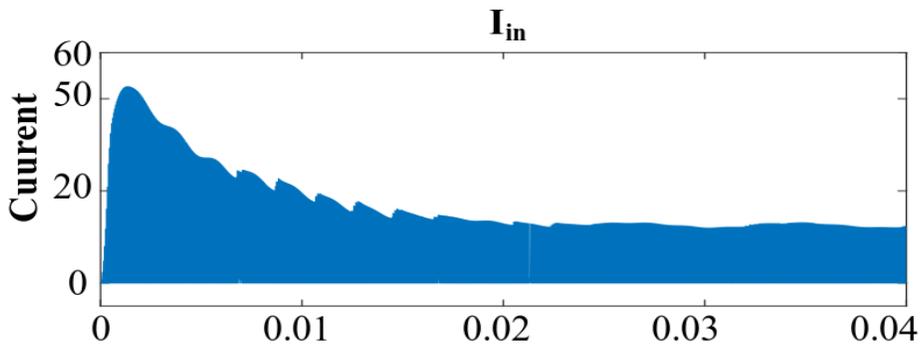
(c)



(d)



(e)



(f)

Figure 5.15 Simulation results. (a) DC-link voltage, (b) output line voltage, (c) output phase voltage, (d) output phase current, (e) capacitor voltages VC1, VC3, and (f) inrush current.

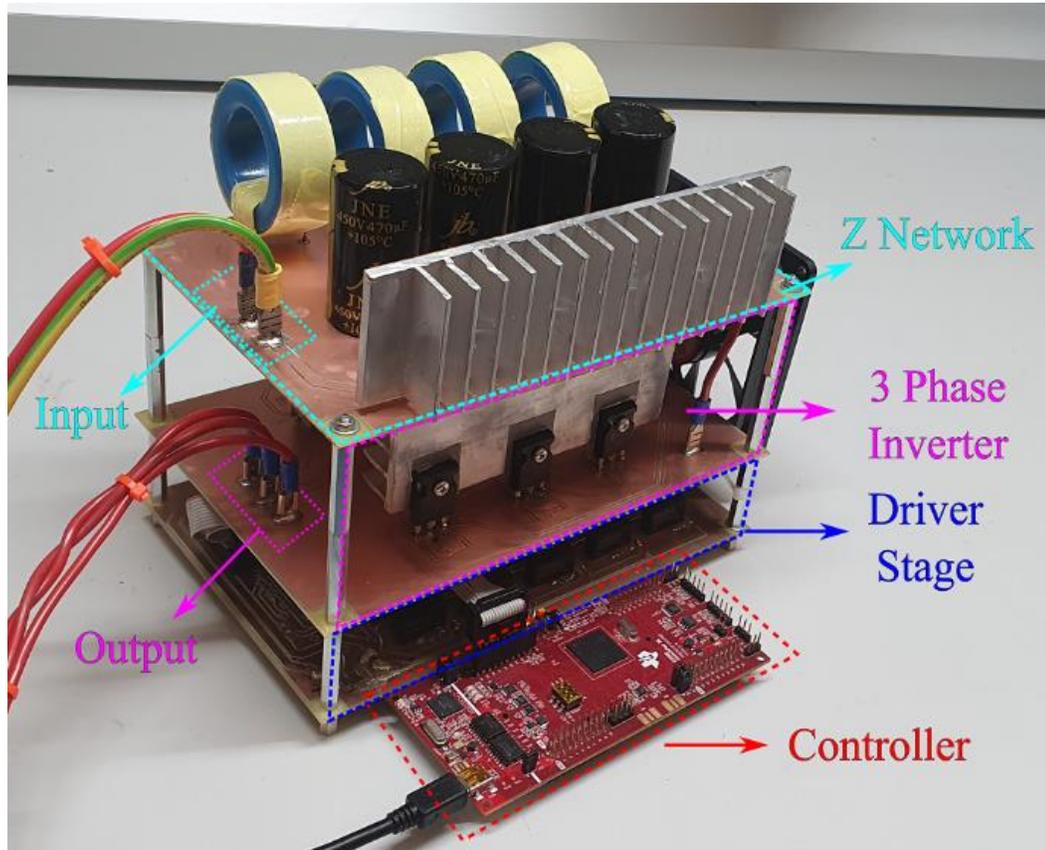


Figure 5.16 Experimental prototype of proposed converter

By using (5.17), (5.18), (5.19), and (5.20), the boost gain is $B = 3.65$, and the buck-boost factor is $G = 3.08$. According to the simulation results, it can be seen that the V_{dc} , V_{C1} and V_{C3} are boosted to 289V, 105V, and 58V, respectively. Furthermore, the peak voltage \hat{V}_{ac} is amplified to 192V.

Table 5.4 Power Loss Calculation Parameters

Inrush current	EB-qZSI	DA-qZSI	HBAS-qZSI	EB-ASqZSI	NN-qZSI	Proposed qZSI
	120A	65A	NO	NO	65A	55A

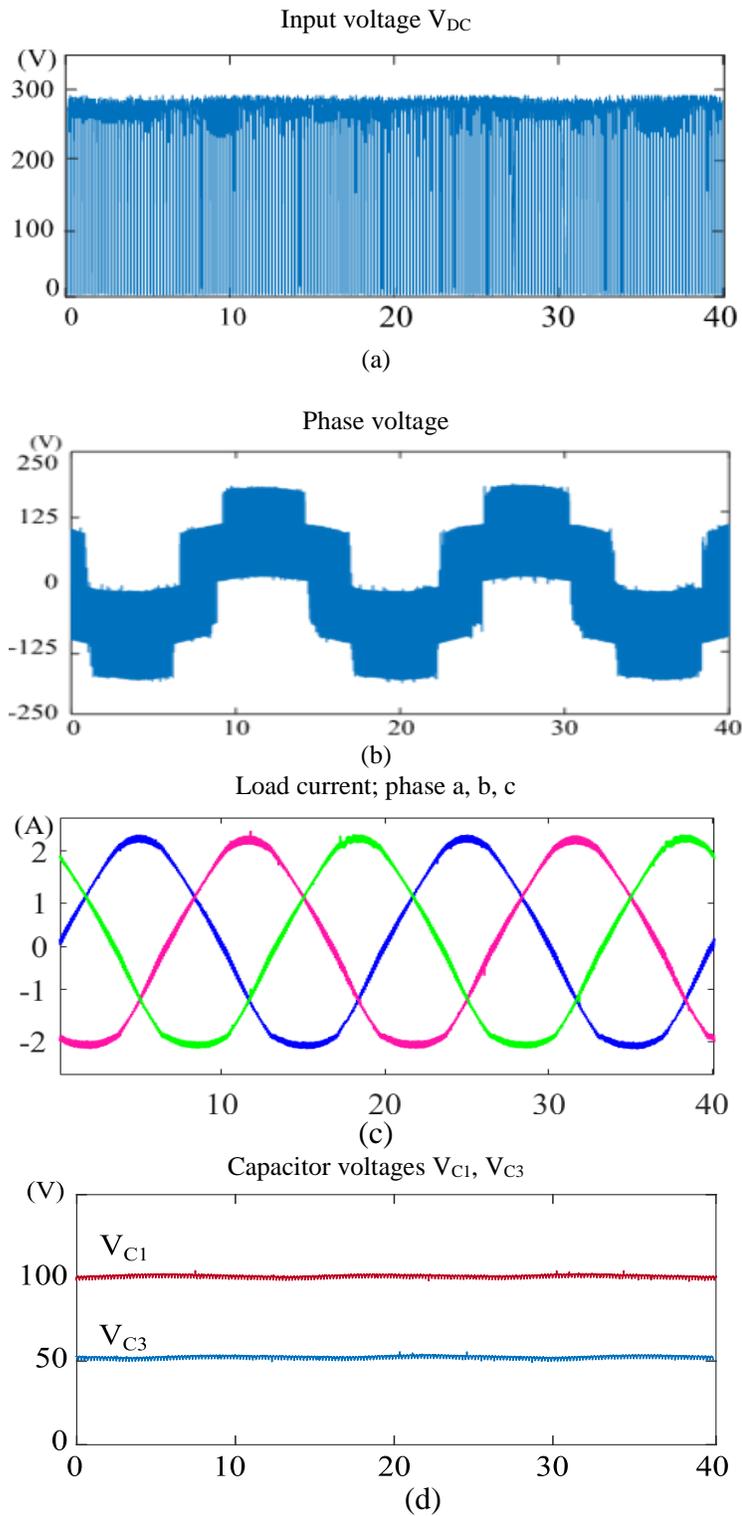
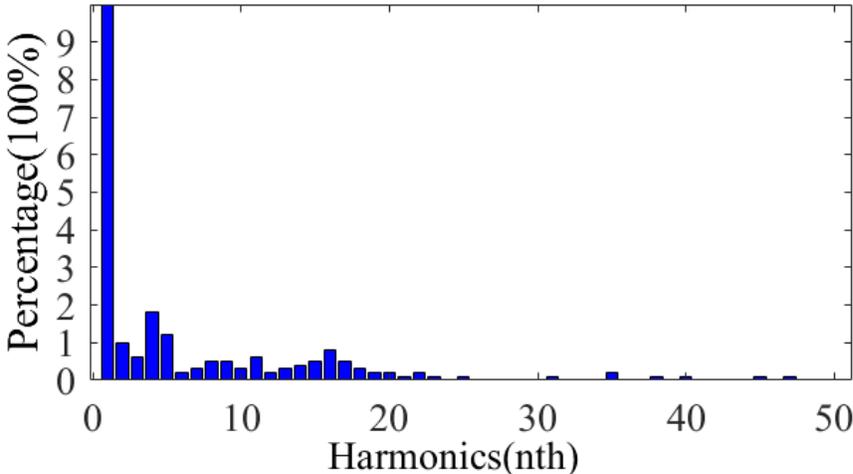
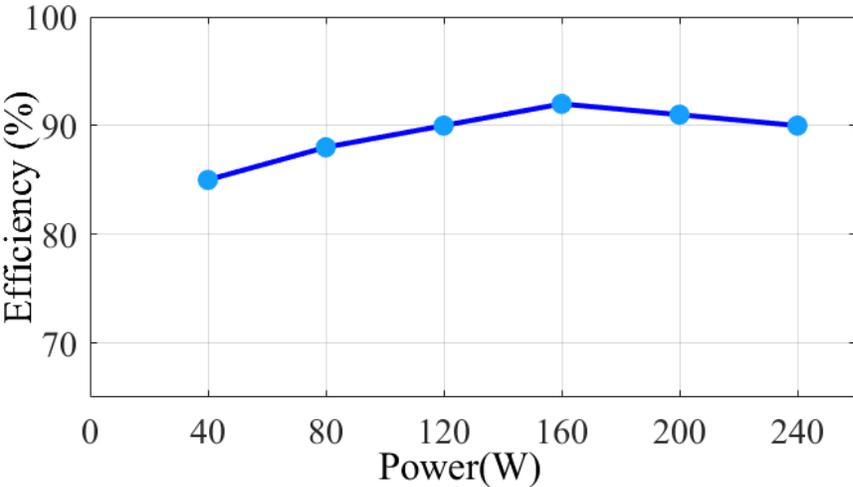


Figure 5.17 Experimental results: (a) input voltage V_{DC} , DC-link (b) output phase voltage, (c) load current, phase a, b, c and (d) capacitor voltages V_{C1} , V_{C3} . ($0 < t < 40\text{ms}$)

Figure 5.16 shows the experimental setup consisting of three main parts: firstly, the control part is based on the C2000 Delfino F28379D (DSP) controller. The driver is the second part, which comprises isolation and negative bias. The last part is the power section, which includes the suggested topology to convert the DC voltage source to AC voltage on the load.



(a)



(b)

Figure 5.18 Experimental results: (a) Measured FFT of the output load current, (b) Measured efficiency versus output power.

Experimental results for the proposed structure inverter at $V_{in}=80V$ and $D = 0.15$ are shown in Figure 5.17. The peak DC-link voltage is illustrated in Figure 5.17(a). According to this figure, the peak DC-link voltage is 286.3V, slightly lower than the theoretical value ($3.65*80=292V$) due to the parasitic parameters of the active elements and passive elements (Inductors, capacitors, diodes, and switches). In Figure 5.17(b), the experimental output phase voltage waveform before filtering is presented. It can be seen in Figure 5.17(b) the peak phase voltage of the AC output is about 190V, which is a little lower than our ideal value because of the parasitic effect of the active/passive components. Figure 5.17(c) shows the three phase load current when an inductive load of $40 \Omega+10mH$ is used. According to Figure 5.17(c), the maximum value of current is 2.3A. The capacitor voltages are measured and shown in Figure 5.17(d), $V_{C1} (=V_{C2})$ are boosted to about 105V and V_{C3} is about 52V.

5.8 Conclusion

In this chapter, a new structure of a Z-source Inverter with a switched network for grid applications presented. In the structure, there was a different impedance network. It was compared with other topologies such as EB-qZSI, DA-qZSI, HBAS-qZSI, EB-ASqZSI, and NN-qZSI. The proposed topology offers high boost factor gain (B) at low shoot through duty ratio (D) and high modulation index (M) to provide a high quality output waveform. Furthermore, the voltage stress across the capacitors is lower compared to other similar converters. Thus, lower voltage rating capacitors can be used to reduce the system's cost, size, and weight. In addition, as in EB-qZSI, the proposed topology mitigates the problem of starting inrush current at start-up conditions. The simulation results and experimental results confirm the advantages and effectiveness of the proposed inverter topology.

Conclusion and future work

Conclusion

The thesis focused on converters, which are the bridge between the renewable energy source, particularly a DC source, and the ac grid. The main goal of the research study was to improve the way to transfer the energy from the PV panels to the grid. Particularly, the research takes advantage of the many low-voltage cells in the PV structure. The idea was to combine efficiently the cells in different ways to create a sinusoidal waveform with low distortion.

In chapter 1, the review of traditional multilevel inverters are studied. From this chapter, can be realized that the use of multi-level inverters has expanded due to the ability to use more than two voltage levels to supply a sinusoidal output voltage. The structure of FC and NPC, which operates on the principle of voltage blocking in power switches via diodes and capacitors, is one of the introduced multi-level topologies. These principles are commonly implemented in industry; however, the necessity to connect the components in series restricts the technology's practical applicability. This chapter compared multi-level topologies with criteria such as the number of isolated dc source components to help designers in choosing the optimal topology. It should be emphasized that there is no difference in the number of switches in three-level topologies between NPCs, FC inverters, and cascaded H-bridge inverters; however, the blocking element and the number of DC sources are different. One downside of the cascaded technique is the requirement for two separate dc sources, whereas the NPC and FC topologies require just one source.

In chapter 2, first introduced traditional impedance source converters; then discussed the details of the converters. The goal of this chapter was to illustrate the various topologies of Z-Source Inverters and to analyze their benefits and drawbacks. Since the switched inductor Z-source concept was initially introduced, many specialists have worked hard and offered. This review described several switched ZSI topologies, architectures, combinations, and models, including the basic switched

inductor ZSI, two-switched inductor/capacitor ZSIs, and active switch boost ZSIs. Switched ZSIs can be configured as single-phase or three-phase inverters regardless of their impedance configuration.

In chapter 3, the literature review for control methods of Multilevel and Z-source converters are investigated. First, many types of carrier-based PWM modulation schemes were presented. The PWM approach is useful for adjusting output voltage and reducing harmonics. There are several modulation strategies that can be implemented for multi-level inverters. Some few modulation methods for multilevel converters were also briefly discussed. Secondly, this chapter provided a more in study of modeling, control, and modulation techniques for impedance source networks for power converters. Modulation methods are generally categorized into 5 groups, with some further subclasses. Furthermore, in order to achieve the maximum voltage boost, the least amount of harmonic distortion, the least amount of semiconductor stress, and the fewest number of device commutations for each switching period, different modulation schemes for specific switching configurations must be compared based on mathematical complexity and performance.

In Chapter 4, a novel multilevel inverter topology for renewable energy sources and industrial loads applications was developed. The suggested topology's basic unit generated 15 levels (output voltage) with fewer components and three DC inputs. The low number of components results in reduced size, a simple control technique, and significant efficiency. The theoretical conduction and switching losses of the proposed 15-level inverter functioning with nearest level modulation were obtained. According to this chapter, connecting basic units in a cascade leads to higher output voltage levels. The suggested topology was compared to a variety of different multilevel topologies. As a result, it showed the advantages of less TVS, reduced number of switches, and fewer DC sources. The simulation and practical results in a 15-level inverter prototype validated the theoretical theory.

In Chapter 5, a new topology of a Z-source inverter with a switched network for grid applications is introduced. There was a different impedance network in the topology. It was compared to various topologies such as EB-qZSI, DA-qZSI, HBAS-qZSI, EB-ASqZSI, and NN-qZSI. The suggested architecture provides a high boost factor gain (B) at a low shoot through duty ratio (D) and a high modulation index (M) to produce a high quality output waveform. Furthermore, the voltage stress across the capacitors was smaller than in other comparable converters. As a result, lower voltage rating capacitors can be utilized to minimize the cost, size, and weight of the system. Furthermore, like with EB-qZSI, the suggested architecture mitigates the problem of initial inrush current during startup. The strengths and performance of the suggested inverter topology were proven by simulation and experimental results.

To sum up the thesis focus was on improving the features of power converters, especially multilevel inverters, and Z-source converters. In the first goal of the thesis, the proposed 15-levels inverter is designed. It has a new structure of a multilevel inverter with fewer components, which is suitable for renewable energy sources and industrial loads applications. Furthermore, it can be connected in a cascade for increasing, even more, the number of levels and output voltage. The main feature of the proposed inverter is its very low harmonic distortion at the output voltage and current due to the control method, which is based on the nearest level control method for generating a high-quality output voltage. A typical application of this inverter is in solar cells and wind turbines. The second goal of the thesis is intended to build a Z-source converter with improved features to compensate the drop voltage of multilevel inverter (when the PV or inputs have a fluctuation). The proposed Z-source structure has a very high voltage boost gain at a low shoot-through duty ratio and high modulation index to reduce the semiconductor stress. Also provides a better-quality output waveform. Furthermore, the proposed structure applies less voltage across its capacitors. Therefore, the installation cost and weight can be reduced by using lower

rating capacitors. Moreover, this suggested structure can also overcome the problem of starting inrush current. Both converters are implemented in the Skoltech laboratory, which verified theoretical outcomes both analytically and in simulation. The obtained theoretical results are also verified experimentally.

Future Work

This work has successfully demonstrated the potential of two new topologies, namely multilevel inverter and Z-source converter for high gain voltage and high power grid-connected applications. In future works, due to having both advantages in one system, such as high gain boost, low stress voltage on the components, low inrush current and low THD output voltage, the combination of multilevel inverter and Z-source converter topologies can be studied.

Figure 6.1 shows the block diagram for the combination of two converters, the application of this connection is to compensate for any drop voltage and work in the MPPT conditions, especially in shading and fluctuating time. This combination has three inputs and one output, which can use renewable energy sources for inputs. For having high-quality output waveform voltages is better to keep constant input voltages. However, the Z-source part can compensate for this drop in voltage quickly. In the application, connecting the Z-source's input to E_1 , E_2 , and E_3 is the same, but the gain factor will change based on inputs.

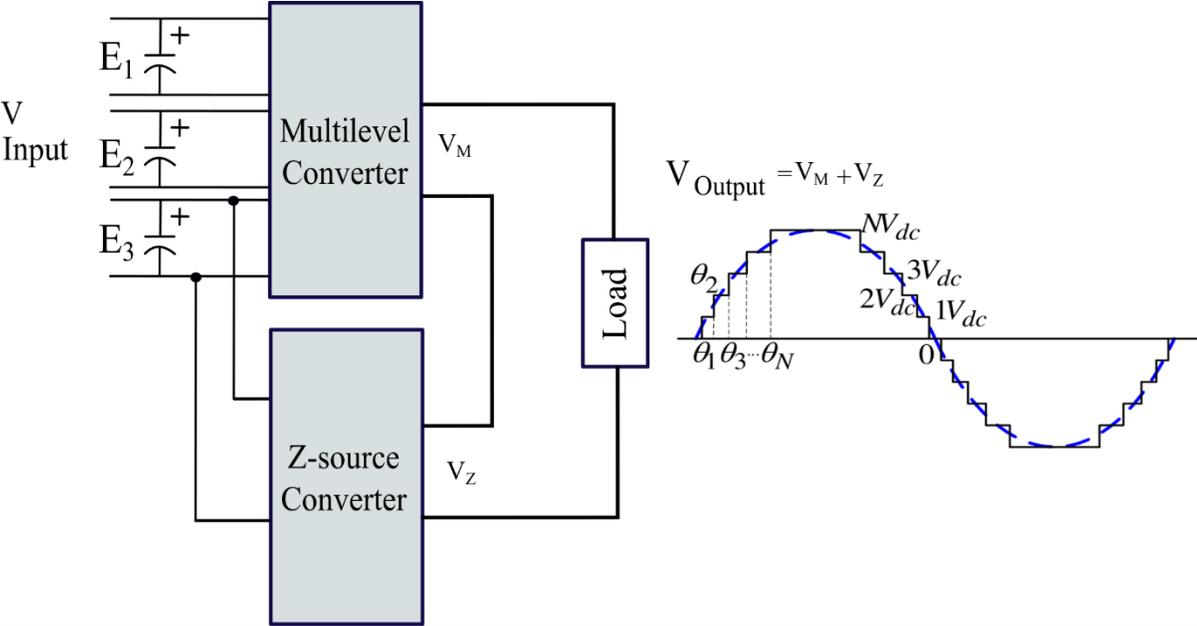


Figure 6.1 Block diagram for combination of two converter (In future works)

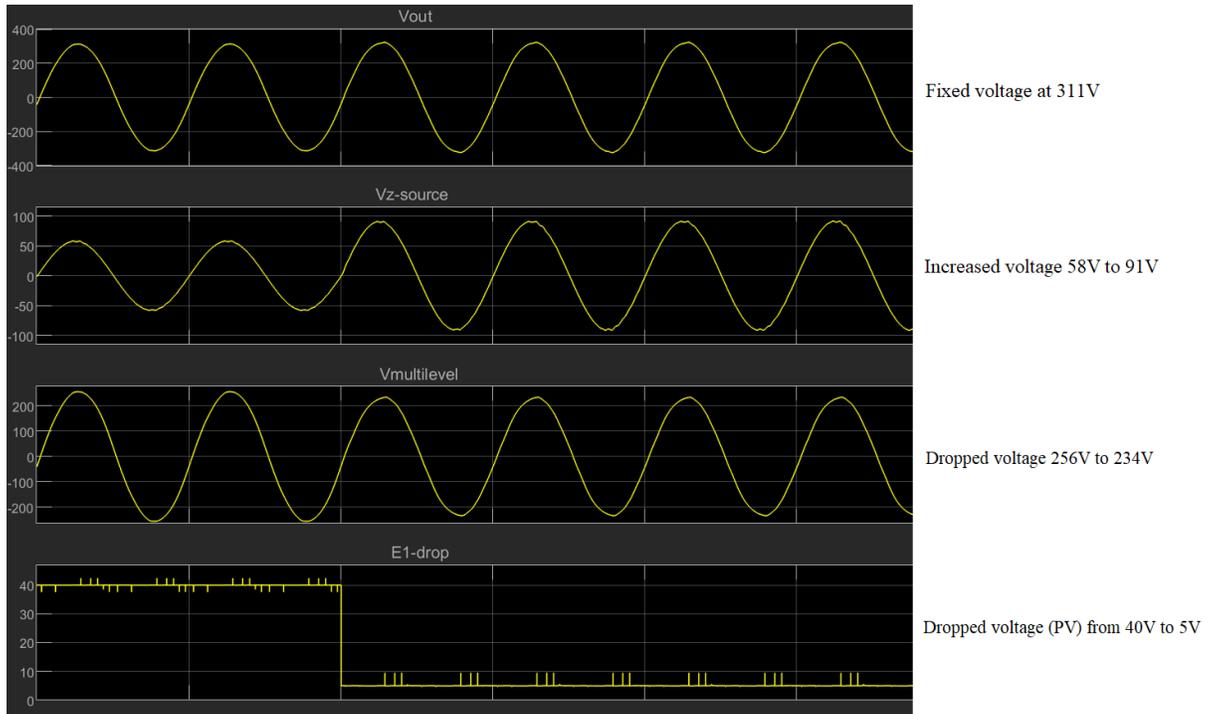


Figure 6.2 Simulation results for combination of both converters in drop voltage (In future works)

For control part, needs to measure all inputs voltages, especially fast tracking in voltage fluctuation. By considering voltage fluctuations, can be compensate the drop voltage with Z-source converter.

Figure 6.2 illustrate the simulation results for the combination of both converters. In this figure, can be seen that the drop voltage is applied for E_1 (40V to 5V) which is one of the inputs for the multilevel inverter, so, due to that the output voltage of the multilevel inverter is reduced from 256V to 234V. To compensate for the drop voltage, the proposed Z-source converter increased its output voltage from 58V to 91V to fix the total output voltage ($V_{Tout}=V_{Mout}+V_{Zout}$) at 311V. For future, the next step is to develop mathematical models for investigating on losses and efficiency. Then can be work on comparison parts, which show advantages and drawbacks of proposed topologies. Finally, the experimental prototype can be carried out to validate the model and mathematical results.

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